Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

THIRD SEMESTER BTECH. (E & C) DEGREE END SEMESTER EXAMINATION

JULY 2021

SUBJECT: ANALOG ELECTRONIC CIRCUITS (ECE - 2151)

TIME: 2 HOURS **MAX. MARKS: 40**

Instructions to candidates

- Answer **ANY FOUR FULL** questions.
- Missing data may be suitably assumed.

1A. The circuit of Fig. 1A must provide a voltage gain of 10 and an input impedance of 100Ω. With I_D = 1.0mA, and $\lambda = 0$, determine the values of R_D and W/L. For the same circuit, suppose I_D = 1.0mA, $\lambda = 0$, and V_b = 1V. Determine the values of W/L and R_D for an input impedance of 100Ω and maximum voltage gain. Use $\mu_n C_{OX} = 100\mu A/V^2$, V_{DD} = 1.8V and V_{TH} = 0.5V.

1B. In Fig. 1B, the MOSFET specifications are, $\mu_n C_{OX} = 100\mu A/V^2$, V_{TH} = 0.5V and $\lambda = 0$. With I_D = 1mA, V_{DD} = 1.8V, and W/L = 100, assuming the current flowing through R_2 to be 1/10 of I_D, calculate the values of R_1 and R_2.

(5+5)

2A. In the circuit of Fig. 2A, V_{DD} = 1.8V, $\mu_n C_{OX} = 100\mu A/V^2$, V_{TH} = 0.5V, I_1 = 0.5mA, R_D = 1kΩ, $\lambda = 0$, and C_1 is very large. i) Compute the value of W/L to obtain a voltage gain of 10 ii) Calculate the values of R_1 and R_2 to place the device 400mV away from the triode region and current through them is no more than 0.1mA iii) With the values found in (ii), what would happen if W/L is twice that found in (a)?

2B. Design a circuit to create copy of currents using MOSFET's from a reference current source of 1mA for the circuits shown in Fig. 2B(i) and Fig. 2B(ii). Assume $\mu_n C_{OX}=100\mu A/V^2$, V_{TH} = 0.5V, $\lambda=0$.

(5+5)

3A. For the circuit shown in Fig. 3A, find

(i) The voltage at node 'X' by viewing 'M_1' as a Common Source stage degenerated by the impedance seen at the source of 'M_2'.

(ii) The voltage at node 'Y' by viewing 'M_1' as source follower and 'M_2' as a common gate stage.

(iii) The differential voltage gain $(V_X-V_Y)/V_{in}$

3B. Consider the circuit shown in Fig. 3B Derive the transfer function assuming $\lambda > 0$ but neglecting other capacitances. Explain why the circuit operates as an ideal integrator if $\lambda \rightarrow 0$.

(5+5)

4A. For the CS stage of Fig. 4A Obtain the expressions for poles of the circuit using Miller's approximation. If R_S = 200Ω, R_L =1 kΩ, I_D = 1 mA, C_{GS} = 50fF, C_{GD} = 10 fF, C_{DB} = 15fF, and $V_{GS}-V_{TH}$ = 200mV, using high frequency model of the transistor, calculate the poles

4B. Determine the sense and return technique and polarity of the feedback for the circuit in Fig. 4B. Assuming $R_1 + R_2$ is very large and $\lambda = 0$, compute the closed-loop gain and I/O impedances.

(5+5)

5A. Design a MOSFET based ring oscillator for generating a sine wave of frequency 2 kHz. Assume only capacitors of 0.1μF are available.

5B. Explain the working principle of class AB amplifier with circuit diagram.

(5+5)

6A For the circuit shown in Fig. 6A, find the voltage gain for 1.8mW power consumption. Also, modify and design the circuit with another MOSFET 'M2' stacked, 1.8V Supply and 1.8mW Power budget to enhance the voltage gain to 10^4. Assume $\mu_n C_{OX}=100\mu A/V^2$, V_{TH} = 0.5V, Over drive voltage of 0.2V, $\lambda=0.1V^{-1}$.

6B Identify the feedback topology in the block diagram shown in Fig. 6B. Find its I/O impedance

(5+5)

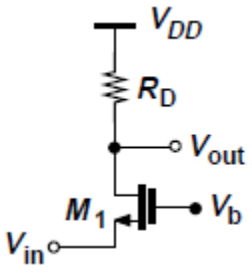


Fig. 1A

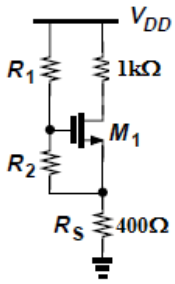


Fig. 1B

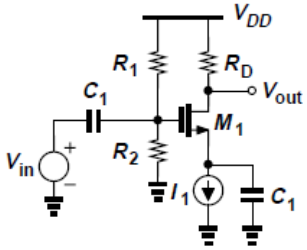


Fig. 2A

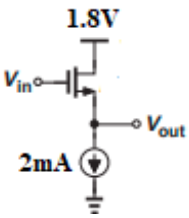


Fig. 2B(i)

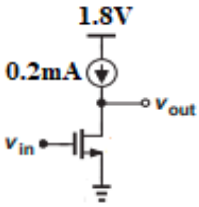


Fig. 2B(ii)

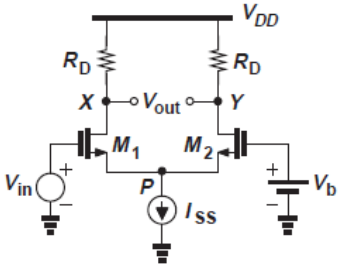


Fig. 3A

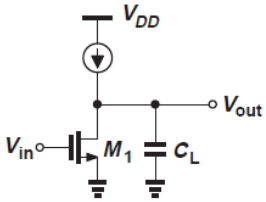


Fig. 3B

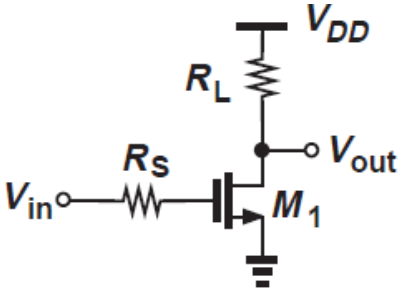


Fig. 4A

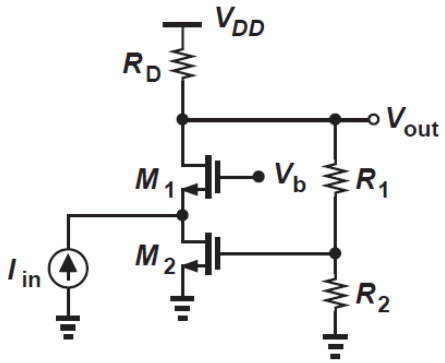
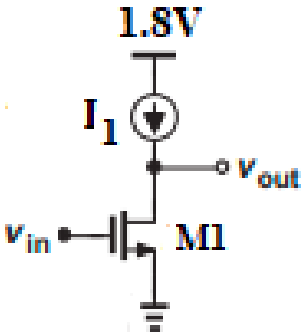


Fig. 4B



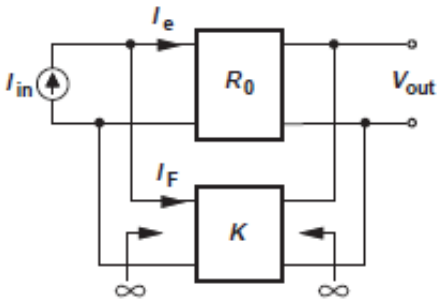


Fig. 6A **Fig. 6B**