Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

THIRD SEMESTER BTECH. (E & C) DEGREE END SEMESTER EXAMINATION
MARCH 2021
SUBJECT: ANALOG ELECTRONIC CIRCUITS (ECE - 2151)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. In Fig. Q1A, the MOSFET specifications are, $\mu_n C_{OX} = 100\mu A/V^2$, W/L = 100, V_{TH} = -0.5V and $\lambda = 0$. Assume capacitor to be large enough to be assumed as short circuit at the operating frequency. Design the amplifier circuit for a voltage gain of 10 and input resistance of 50kΩ. With V_{DD} = 1.8V, R_S = 100Ω, and voltage drop across R_S is 400mV. If a 8Ω speaker is connected at the output, what would be the new gain? What additional changes you suggest if the gain should remain undisturbed?

1B. In the circuit of Fig. Q1(B1) MOSFET spefications are, $\mu_n C_{OX}=100\mu A/V^2$, W/L=10, V_{TH}=0.5V and λ=0.

i. If V_1 is varied from 0 to 1.8V, plot drain current as function of V_{DS}.

ii. What would happen to drain current if V_1 is varied from 0 to 1.8V with connections as seen in Fig. Q1(B2).

1C. There are 6 MOSFETs with the specfications shown in the table. Rest of the spefications are, $\mu_{nSi}=1350cm^2/(Vs)$, $\mu_{pSi}=480cm^2/(Vs)$, $\varepsilon_{Si}=11.7$, $\varepsilon_0=8.85\times10^{-14}$ F/cm, $\varepsilon_{SiO2}=3.9$, tox = 50nm, $|V_{THn}|=|V_{THP}|=0.5V$, $\gamma = 0.4\sqrt{V}$ and $\phi_F = 0.4V$. Which device has the highest drain current flowing through it?

	Type	W(μm)	L(μm)	$\lambda(V^{-1})$	V_G(V)	V_S(V)	V_D(V)	V_B(V)
1	PMOS	10.00	1	0.10	1.0	-0.5	1.0	-0.5
2	PMOS	10.00	10	0.01	1.5	0.5	1.5	0.5
3	NMOS	3.55	1	0.10	1.5	0.0	1.5	0
4	NMOS	3.55	10	0.01	1.0	-0.5	1.0	0
5	PMOS	15.00	1	0.01	0.5	-0.5	1.0	-0.5
6	NMOS	15.00	1	0.10	1.0	0.5	1.5	0.5

(4+3+3)

2A. In the circuit of Fig. Q2A, $\mu_n C_{OX} = 200\mu A/V^2$, $\mu_p C_{OX} = 100\mu A/V^2$, $W/L_{M1} = 10$, $W/L_{M2} = 20$, $|V_{TH}| = 0.5V$ and $\lambda = 0$. i) Plot the drain currents (I_X and I_Y) as a function of V_B with V_B varrying between 0 to 1.5V. If required, assume V_{DS} to be 1.8V. ii) Repeat (i) with both devices considered to be NMOS. (iii) in case (ii), when the scenario is non ideal, of the two resulting drain resistances (R_{DSM1} and R_{DSM2}), which one will be higher? Why?

2B. For the Cascode amplifier shown in Fig. Q2B, $(W/L)_1=30$, $(W/L)_2=40$, $I_1=0.5$ mA. If $\mu_n C_{ox}=100\ \mu A/V^2$, $\lambda_n=0.1\ V^{-1}$, determine the voltage gain.

2C. Determine the current I_{copy} in the circuit shown in Fig. Q2C.

(4+3+3)

3A. For the circuit shown in Fig.Q3A, for the half circuit determine:
i. Differential gain ii. Common mode gain and iii. CMRR.
Assume the inputs V_1 and V_2 as small ac signals, 'M1' and 'M2' as identical MOSFETs, $\mu_n c_{ox} = 100\mu A/V^2$ and $\lambda=0$.

3B. Assuming $\lambda > 0$ and using Miller's theorem, determine the input and output poles of the stage depicted in Fig. Q3B.

3C. With the help of small signal model, derive the expressions for high frequency poles of CS stage

(4+3+3)

4A. Find the closed loop gain, I/O impedance of the circuit shown in Fig. Q4A.

4B. Determine the sense and return technique and polarity of the feedback for the circuit in Fig. Q4B.

4C. Derive an expression for efficiency of Class B push - pull power amplifier.

(4+3+3)

5A. Explain the working of Ring Oscillator with a neat circuit diagram. Obtain the expressions for gain and frequency of oscillation.

5B. Determine the gain and output impedance for the circuit shown in Fig. Q5B. Assume $\lambda>0$.

5C. Starting from drain current expression derive the small signal model of MOSFET.

(4+3+3)

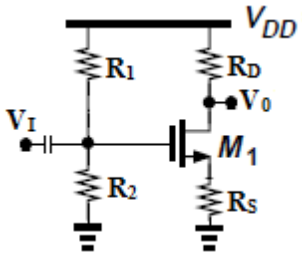

Fig. Q1A

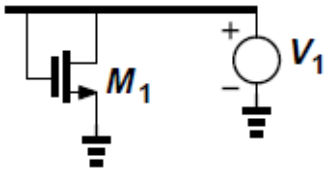

Fig. Q1(B1)

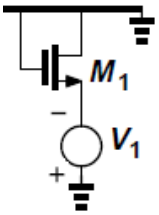

Fig. Q1(B2)

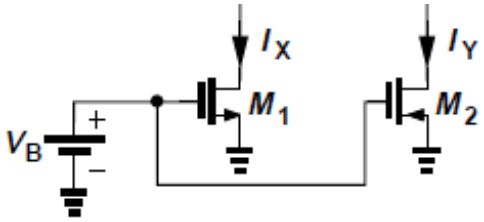

Fig. Q2A

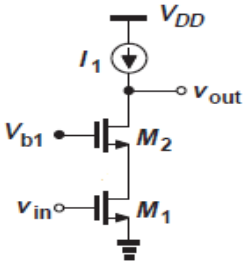

Fig. Q2B

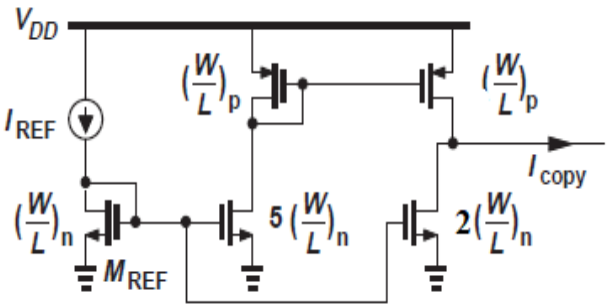

Fig. Q2C

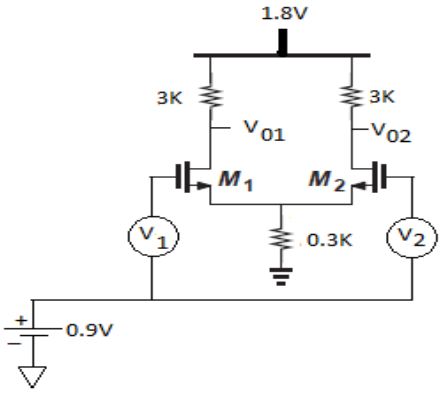

Fig. Q3A

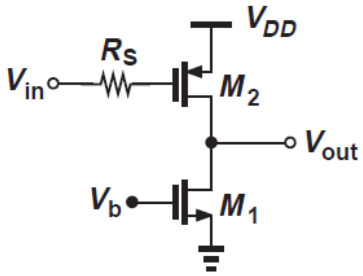

Fig. Q3B

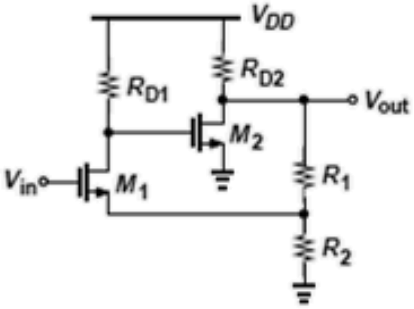

Fig. Q4A

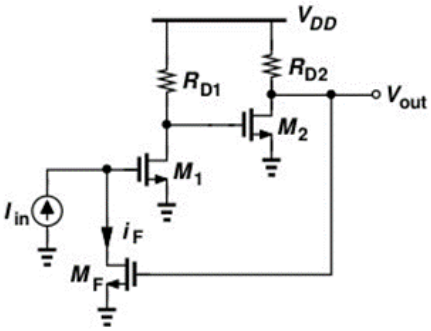

Fig. Q4B

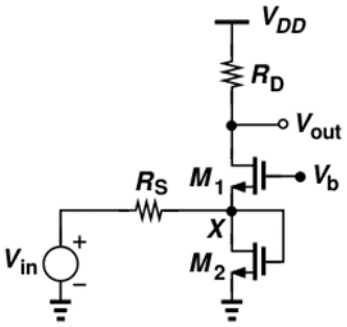

Fig. Q5B