Exam Date & Time: 10-Mar-2021 (09:00 AM - 12:00 PM)

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

THIRD SEMESTER B.TECH (ELECTRONICS AND INSTRUMENTATION ENGG.)
END SEMESTER EXAMINATIONS, MARCH 2021

DIGITAL ELECTRONICS CIRCUITS [ICE 2152]

Marks: 50 **Duration: 180 mins.**

A

Answer all the questions.

Instructions to Candidates: Missing data may be suitably assumed

1) Define any four performance matrices of logic families. (2)

A)

B) How is an error detecting code different from an error correcting code? Encode data bits 0111 into 7 bit even parity hamming code. Decode the received hamming code message '0011011' assuming that single error has occurred. (3)

C) Using QM method, obtain the minimal expression for the function, $f = \prod M(1,4,5,11,12,14).d(6,7,15).$ Implement it in universal logic. (5)

2) Design a circuit to detect the numbers 0, 1, 4, 6, 7 and 8 in a 4 bit XS - 3 code input. Implement it using universal logic. (4)

A)

B) With neat circuit diagram, design a 2-bit magnitude comparator. (3)

C) Design a half - subtractor using NOR logic. (3)

3) Realize the logic expression, $f = \sum m\,(2,4,5,7,9,10,14,15)$ using (i) 8:1 MUX, (ii) 4:1 MUX. (4)

A)

B) Design a basic 10 – line to 4 – line encoder circuit. (3)

C) With suitable logic diagram, explain the function of Twisted Ring Counter. Also draw its timing diagram. (3)

4) The input signals shown in Fig.Q4A are applied to an S-R flip flop with active - high PRESET and CLEAR. Draw the output waveform for a positive and negative edge triggered S-R flip-flop. Assume that the present state of flip flop is '0'. (2)

A)

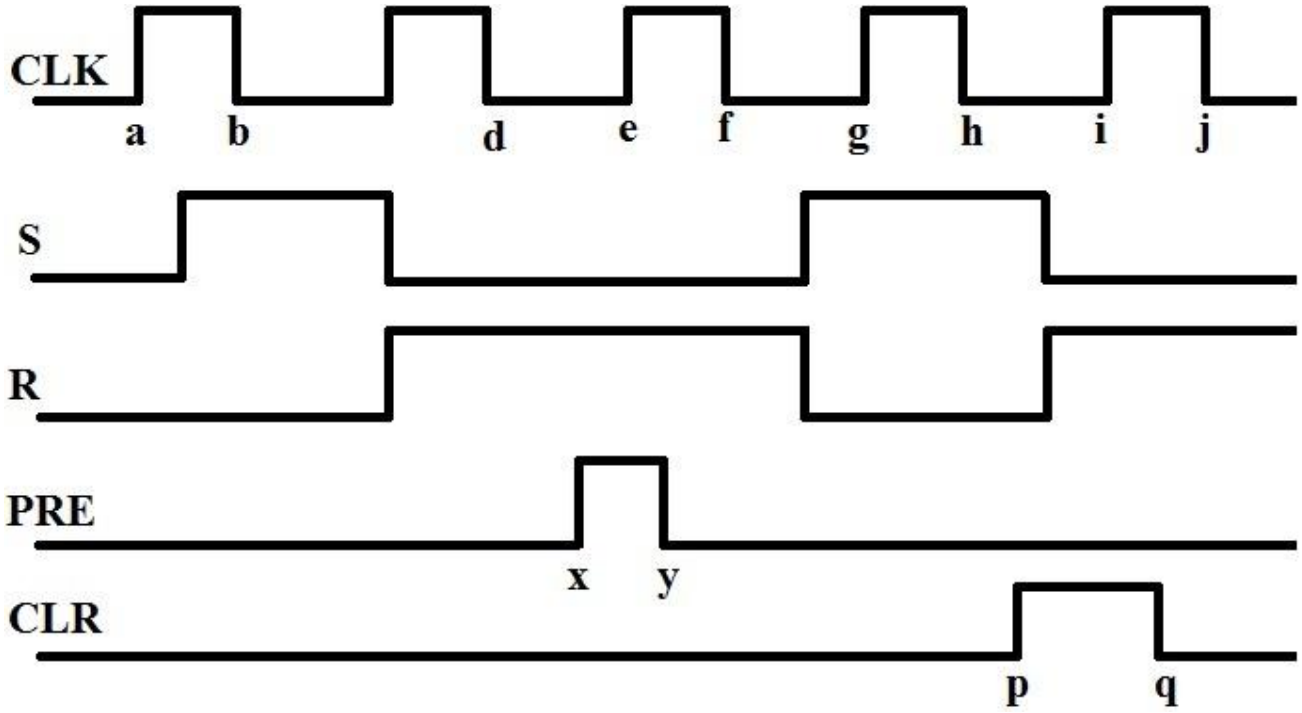

Fig.Q4A

B) Design a cyclic counter using T flip flop that counts 2, 6, 7, 11, 12, 13, 2, 6 ... and unused states of the counter change to 7 at the next clock pulse. (5)

C) An asynchronous sequential circuit is described by the excitation and output functions

$$Y_1 = x_1x_2 + x_1y'_2 + x'_2y_1$$

$$Y_2 = x_2 + x_1y'_1y_2 + x'_1y_1$$

$$z = x_2 + y_1$$

(3)

Derive the transition table and output map. Draw the logic diagram of the circuit.

5) A clocked sequential circuit with single input x and single output z produces an output z = 1 whenever the input x completes the sequence 1101 with overlapping allowed. Obtain the state diagram and design the circuit with D flip flops for a Mealy type sequence detector. (5)

A)

B) Draw an ASM chart and state table for a 2-bit up-down counter having mode control input,
M = 1: Up counting

M = 0: Down counting

The circuit should generate an output '1' whenever the count becomes either minimum or maximum. (3)

C) Describe the critical race condition in asynchronous sequential circuit with suitable example. (2)

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