Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

DEPARTMENT OF MECHATRONICS ENGINEERING

III SEMESTER B.TECH. (MECHATRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, March 2021

SUBJECT: DIGITAL SYSTEM DESIGN [MTE 2152]

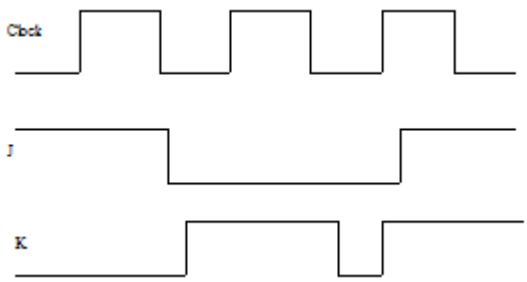
5/3/2021

Time: 3 Hours **MAX. MARKS: 50**

Instructions to Candidates:

- Answer **ALL** the questions.

Q. No		M	CO	PO	LO	BL
1A.	Obtain i) minimal SOP ii) minimal POS expression using K-map for the following equation. $\mathbf{f(A,B,C,D)=\sum m(0,2,4,5,6,15)+d(3,7,8,9,10,13)}$	**4**	**1**	**PO1 PO12**	**1, 7, 13**	**3**
1B.	Implement the four Boolean functions listed below using three half adder circuits. $D = A \oplus B \oplus C$ $E = \overline{A}BC + A\overline{B}C$ $F = AB\overline{C} + (\overline{A} + \overline{B})C$ $G = ABC$	**4**	**2**	**PO1 PO2 PO12**	**2,7, 9, 13**	**3**
1C.	Using 74283 develop a 4 bit Binary to Excess 3 code converter	**2**	**2**	**PO1 PO3 PO12**	**2,7, 9, 13**	**3**
2A.	Realize the Boolean expression $f(w,x,y,z) = \sum m(0,2,4,5,7,9,10,14)$ Using a multiplexer tree structure. The first level should consist of two 4-to-1 line multiplexers with variables w and z on their select lines S1 and S0 , respectively, and second level should consist of a single 2-t0-1 line multiplexer with the variable y on its select line.	**4**	**2**	**PO1 PO3 PO12**	**2,7, 9, 13**	**2,3**
2B.	Write a behavioral Verilog Code for a 1 bit full adder. Using this as a component write a Verilog code for a 4 bit full adder.	**4**	**5**	**PO1 PO5 PO12**	**6,7, 8, 18**	**1,3**
2C.	Which are the asynchronous inputs of Flip Flops? State their importance.	**2**	**3**	**PO1 PO12**	**3,7, 8,9, 13**	**1**

3A.	Design and implement a 4 bit even number generator using T flip flops.	**4**	**3**	**PO1 PO2 PO3 PO12**	**3,7, 8,9, 13**	**3**
3B.	Construct a JK flip flop using a D flip flop, a 2 to 1 multiplexer and an inverter.	**4**	**3**	**PO1 PO3 PO12**	**3,7, 8,9, 13**	**3**
3C.	Design a Divide by 10 counter using IC 7493	**2**	**3**	**PO1 PO2 PO3 PO12**	**3,7, 8,9, 13**	**3**
4A.	Design a 3 bit gray code down counter using D flip flops.	**4**	**3**	**PO1 PO2 PO3 PO12**	**3,7, 8,9, 13**	**3**
4B.	Define a Programmable Logic Device. List the classification and explain each of them.	**4**	**4**	**PO1 PO6 PO12**	**3,7, 8, 13**	**1**
4C.	Design an asynchronous counter to count from 4 to 12 using T flip flops.	**2**	**3**	**PO1 PO2 PO3 PO12**	**3,7, 8,9, 13**	**3**
5A.	Using a 4 bit universal shift register (74LS194) design a sequence generator which cycles through the following sequence. 0-8-12-6-13-11-7-3-1-0	**6**	**3**	**PO1 PO2 PO3 PO12**	**3,7, 8,9, 13**	**3**
5B.	List the different levels of modelling in Verilog	**2**	**5**	**PO1 PO5 PO12**	**6,7, 8, 18**	**1**
5C.	For the inputs specified sketch Q_M and Q_S of the given flip flop. Consider a –ve edge triggered flip flop. 	**2**	**3**	**PO1 PO12**	**3,7, 8,9, 13**	**1,3**