Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

(A constituent unit of MAHE, Manipal 576104)

IV SEM B.Tech.(BME) DEGREE GRADE IMPROVEMENT EXAM JANUARY 2021
SUBJECT: DIGITAL SYSTEM DESIGN (BME 2253)
(REVISED CREDIT SYSTEM)
Tuesday 12th January, 2021: 2 PM to 5 PM

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to Candidates:

1. **Answer all the questions.**
2. **Draw labeled diagrams wherever necessary.**

1.	(a)	Illustrate the benefits of fully customized ASICs. Compare the architecture of channeled and channel less gate array ASICs.	03
	(b)	Design 2: 1 MUX using transmission gates and inverter. Explain its operation.	04
	(c)	Design a CMOS circuit to realize the following function: F= (A+B)C. Draw the circuit and verify the operation.	03
2.	(a)	Design a 4x4 multiplier using the required number of full-adder and basic gates. Estimate the multiplication time. (when Tc>Ts), where Ts= propagation delay of sum, Tc= propagation delay of carry, Ta= delay of AND gate. Draw the multiplier circuit.	03
	(b)	Design a positive enabled transmission gate latch. Explain its operation with a neat diagram which includes: clock signal with latch input (D), and latch output (Q).	04
	(c)	Design the NMOS AND-OR plane in cases of a PLA for realizing the following function: F1=AC+B'. Sketch the planes and label it.	03
3.	(a)	Describe the typical architecture of FPGA. Contrast the advantages of FPGA over CPLD.	04
	(b)	Construct a two variable LUT based circuit of FPGA for realization of the given function: Y= AB+CD'	03
	(c)	Explain how NMOS based volatile technology is used for the design of a switching circuit in the programmable device.	03

4. (a) Differentiate PAL from PLA. Explain its extended cell of PAL for choosing different data path. 03

(b) Apply Shannon's expansion theorem and write co-factors for the given function (f): f=w1w2w3' +w1'w2w3+w1w2'w3. Synthesis the function using: i) 2:1 multiplexer and basic gates (with respect to variable w2); ii) 4:1 multiplexer and gates if required (with respect to w1w2). 04

(c) Write a Verilog HDL code to synthesis the following function using dataflow modeling style: F= A + (B.C) 03

5. (a) Design a Verilog HDL module to synthesis a 1-bit full adder, using structural style. Consider A, B and C_{in} as input ports S and C_{out} as output ports. 03

(b) Describe the two syntaxes used for creating instance of a module. Create an instance for the 1 bit full adder module named as "full adder" with each of the above syntax. 04

(c) Design of a negetive edge triggered DFF using always statement. 03