Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

FOURTH SEMESTER BTECH. (E & C) DEGREE IN-SEMESTER EXAMINATION
AUGUST 2021
SUBJECT: VLSI DESIGN (ECE - 2254)

TIME: 2 HOURS **MAX. MARKS: 40**

Instructions to candidates
- Answer **ANY FOUR** questions.
- Missing data may be suitably assumed.

1A. Derive the pull-up to pull-down ratio for an NMOS inverter driven through one pass transistors and one transmission gate as shown in **Figure 1A**.

1B. Derive the equation for drain current of NMOS transistor.

(5+5)

2A. A set of I-V characteristics of an NMOS transistor at room temperature have been enumerated in **Table 2A** for different biasing conditions. Using data, Solve for threshold voltage and Electron mobility. Given, W/L= 1, Tox= 300 Å.

Table 2A

VGS	VDS	VSB	ID(μA)
4	4	0	200
5	5	0	400

2B Calculate I_D and V_{SD}, and indicate the region of operation of transistor M_1 for the circuit in **Figure 2B**. Vtp = –0.4 V, Kp =μp*Cox= 120 $\mu A/V^2$, and W/L = 2.

(3+7)

3A. Consider a CMOS inverter with the following device parameters shown in **Table 3A.**

Table 3A

Parameter	NMOS	PMOS
μC_{ox}	60 $\mu A/V^2$	20 $\mu A/V^2$
V_{th}	0.6 V	- 0.8 V
$V_{dd} = 3\ V, V_{ss} = 0\ V$		

Determine the ratio of $\frac{L_n/W_n}{L_p/W_p}$ with switching threshold voltage 1.5 V. and draw the transfer characteristic when Vdd changes to 4 V.

3B. Write ten differences between CMOS technology and Bipolar Technology.

(5+5)

4A. Explain the working of an enhancement type NMOS transistor in cut- off, linear and saturation region. Plot the current-voltage characteristics.

4B. Identify the steps require for the fabrication of CMOS P-well process with neat diagram and explain. Draw the schematic of parasitic latch-up circuit developed in CMOS P-well process.

(5+5)

5A. Consider a 2:4 decoder with inputs A, B and outputs D3, D2, D1, D0. Outputs are active high signal. Given, variables, complement of variables and inputs logic '1' and '0' are available to designer. Implement the 2:4 decoder with NMOS pass transistors with proper interconnections.

5B. Explain the problems associated with first generation of BICMOS inverter. Also, Implement three input majority function using BiCMOS gate logic.

(6+4)

6A. Consider a pseudo NMOS inverter driving another pseudo NMOS inverter. What will be the conditions of PMOS and NMOS transistor around the inverter threshold? What will be the new pull-up to pull-down ratio in the case of pseudo NMOS inverter if $\mu_n=\mu_p$?

6B. Implement logic function $F = \overline{a + \overline{b + \overline{c}}}$ using pseudo NMOS gate logic and CMOS switch logic.

(5+5)

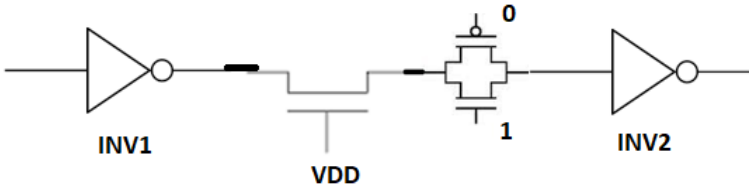

Figure 1A

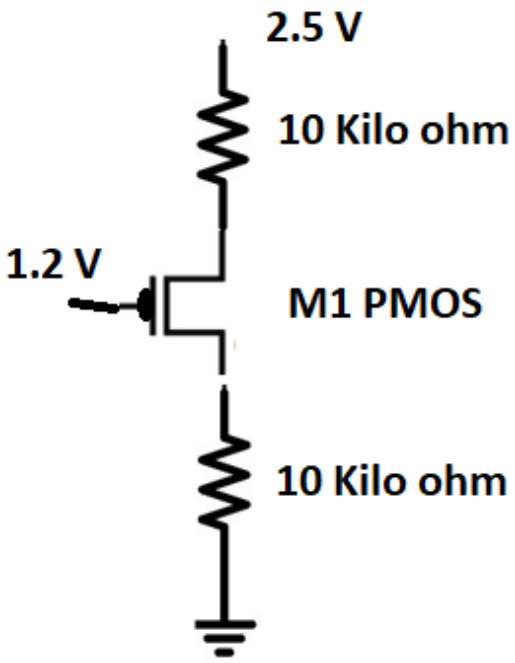

Figure 2B