Reg. No. | | | | | | | | | | |

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

FOURTH SEMESTER B.TECH. (ELECTRONICS & INSTRUMENTATION ENGG.)
ONLINE GRADE IMPROVEMENT/MAKE-UP EXAMINATIONS, AUGUST - 2021

DIGITAL SYSTEM DESIGN [ICE 2251]

13-08-2021

TIME: 2 HOURS **MAX. MARKS: 40**

Instructions to candidates

- Answer **ANY FOUR FULL** questions.
- Missing data may be suitably assumed.

1A. Develop a sequence detector along with circuit to detect the sequence 1101. Write a behavioural code for the same. **6**

1B. Realize the circuit developed in Q1A in Verilog using structural style. **4**

2A. Write a configurable Verilog code that takes an input clock of 10MHz and depending on the configuration sets the output to 2MHz or 4MHz or 6MHz or 8MHz. **5**

2B. Given a crystal frequency of 50MHz, a Verilog code is developed to generate a pulse train of 4ms. Draw the timing diagram for the same. The signals expected in the figure are – system clock, reset, counter, output. Mathematical calculations to support the solution is expected. **5**

3A. Develop a 4bit BCD up-counter using D Flip-Flop (DFF) using structural coding. Implement the DFF (positive edge triggered with active low reset) using UDP. **5**

3B. Illustrate operator precedence with examples. **5**

4A. Find a minimum-row PLA table and diagram to implement the following equations: **5**

X (A, B, C, D) = Σm (0, 1, 4, 5, 6, 7, 8, 9, 11, 12, 14, 15)

Y (A, B, C, D) = Σm (0, 1, 4, 5, 8, 10, 11, 12, 14, 15)

Z (A, B, C, D) = Σm (0, 1, 3, 4, 5, 7, 9, 11, 15)

Write two difference between PLA and PAL

4B. Explain design flow for ASICs based system design, highlighting outcome from in each step. **5**

5A. Explain the programming technologies used to make the FPGAs field programmable. **5**

5B. Sketch the basic block diagram of Xilinx Spartan IIE FPGA. Also explain the major configurable elements briefly. **5**

6A. Determine the necessary inputs to the following network **(Fig.6A)** to test for **5**

i) b stuck at 0 ii) g stuck at 1.

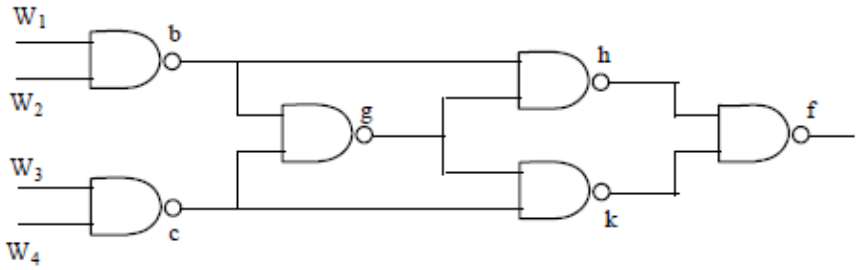

Fig. 6A

6B. Explain logic element and operating modes available in Altera MAX-II FPGA. Explain the technology used to make it field programmable. **5**