Question Paper

Exam Date & Time: 12-Jan-2021 (02:00 PM - 05:00 PM)

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

FOURTH SEMESTER B.TECH END SEMESTER EXAMINATIONS, JAN 2021

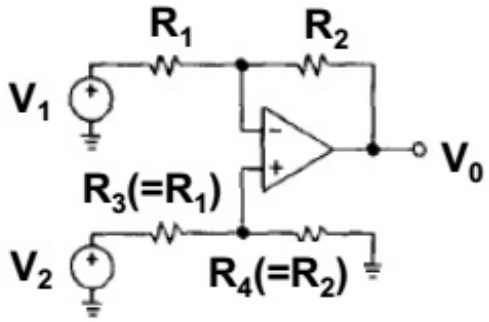
LINEAR INTEGRATED CIRCUITS [ICE 2254]

Marks: 50 **Duration: 180 mins.**

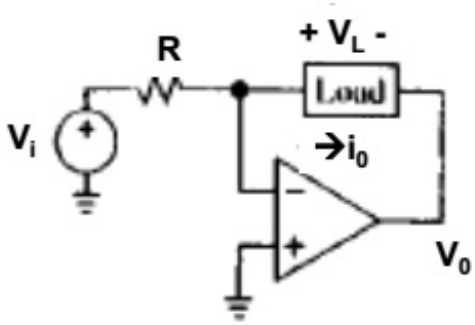
Answer all the questions.

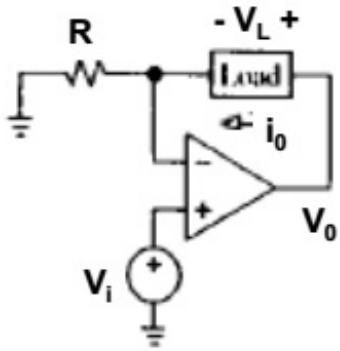
1) Design an OpAmp circuit for amplifying the output of a sensor from 8mV to 4V. (2)

2) Prove that the circuit shown below responds to only differential input and reject common mode input .Also find the expression for the CMRR in db. (4)

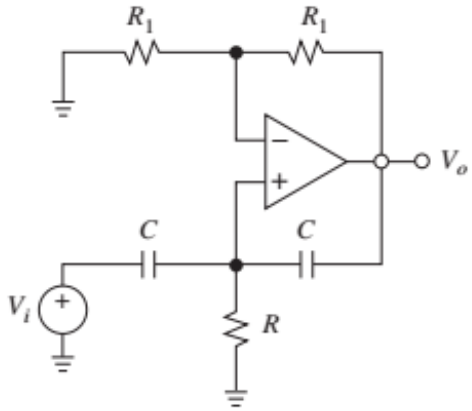


3) Compare the V to I circuits in Figures. Calculate i_o in both cases and find out the voltage compliance and maximum permissible value of load resistance. (4)





4) Obtain component values of the following circuit for a unity-gain frequency of 100 Hz: (2)



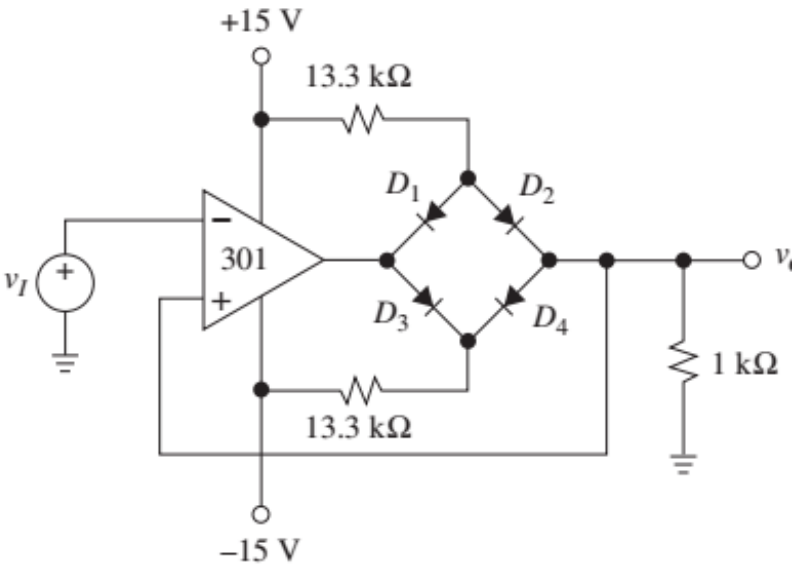
5) Discuss the significance of (i) dominant pole frequency (ii) gain bandwidth product in filter design. (3)

6) Design a second order low pass filter with a higher cut off frequency of 1KHz. Draw the frequency response of the filter. (5)

7) A square wave pulse of 10µs time period is applied to two OpAmps, one with a slew rate of 0.5V/µs and the other with a slew rate of 1V/µs. Plot the output waveform of both the OpAmps (2)

8) Derive the design equations for a Weinbridge Oscillator. (4)

9) Assuming V_D(on)=0.7V and ±Vsat=±13V, comment on the working of the inverting Schmitt trigger of Figure shown and sketch the VTC . (4)



10) Draw a peak-to-peak detector, that is, a circuit that gives $v_O = v_I(max) - v_I(min)$. (2)

11) Design an OpAmp square wave generator for generating signal with frequency varying from 1KHz to 5KHz. (4)

12) Discuss the internal architecture of a 555 timer. (4)

13) The basic step of a 9-bit DAC is 10.3mV. If 000000000 represents 0V, what will be the output of DAC for a digital input of 101101111? (2)

14) With a neat circuit diagram, explain working of a D/A convertor using R-2R ladder circuit. (4)

15) Describe the architecture of 566 Voltage Control Oscillator and its importance in 565 Phase Locked loop. (4)

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