Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

VI SEMESTER B. TECH (ELECTRICAL & ELECTRONICS ENGINEERING)
GRADE IMPROVEMENT EXAMINATIONS, January 2021
EMBEDDED SYSTEM DESIGN [ELE 4001]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 07, January 2021** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Describe how the processing power of a processor is improved using following techniques
   i. Pipeline architecture
   ii. Multicore processors (Parallel processing) ***04***

1B. Write PIC16F877 assembly program to
   i. Configure port 'C' as input port
   ii. Configure pins RB0-RB2 as input pins, RB3-RB5 as output pins and RB6-RB7 as input pins.
   iii. Turn on/off the LEDs connected to pins RA0 and RA1 alternately, continuously, with a suitable delay. ***04***

1C. Write ARM7 assembly program to copy 600, 16-bit data available in successive memory locations starting at 0x00005000 to successive locations starting at 0x00006000 ***02***

2A. Write an ARM7 subroutine for division of unsigned 32-bit numbers. Assume that the dividend and divisor are passed to subroutine through registers R0 and R1 respectively. Return the result through R2(quotient) and R3(remainder). In case attempt to divide by zero, return back with 01 as error code in R4 register. If it is a 0/0 case, return back with 02 as error code in R4 register. ***03***

2B. Write equivalent ARM7 assembly program for the following 'C' code. Use registers R3, R4 and R5 for variables i, j and k and starting memory addresses of array a, b and c as 0x00008000, 0x00009000 and 0x0000A000 respectively.

```
unsigned int a [500] = {0x0000AABB, .....};
unsigned int b [500] = {0x00008899, .....};
unsigned int c [500] = {0x00000000, .....};
unsigned int d [500] = {0x00000000, .....};
unsigned int e [500] = {0x00000000, .....};
    for (i=0; i<500, i++)
    {
       c[i] = a[i] +b[i];
       d[i] = a[i]*b[i];
       e[i] = - a[i];
    }
```

04

2C. Write a technical note on undefined instruction exception in ARM7 processor. ***03***

3A. Write a 'C' program for mbedNXPLPC1768 microcontroller to configure GPIO pins p10 and p111 as rising and falling edge triggered interrupts respectively and wait for the interrupt. When interrupted through p10, write an ISR to obtain a 30%duty cycle, 500Hz waveform at pin p12. When interrupted through pin p11, write an ISR to obtain a 60% duty cycle, 250 Hz waveform at pin p13. ***03***

3B. Answer the following with respect to cache memory

i. Need for cache memory
ii. Levels of cache memory
iii. Draw the memory hierarchy diagram in a system with 2 levels of cache and with separate instruction and data cache at level 1. Explain the (instruction fetch) code memory read operation in such a system.

04

3C. What are handshake signals? Explain the handshake protocol for write operation. List the merits and demerits of handshake protocol by comparing it with strobe protocol. ***03***

4A. Write a 'C' program for PIC16F877 to configure MSSP in SPI master mode to transmit data bytes 3AH and 4B to slave device 1 connected to RC3 pin and then transmit data bytes 5CH and 6DH to slave device 2 connected to RC4 pin. Store the (simultaneously) received data bytes from slave device 1 and 2. Use baud rate of 250 kbps, low state as idle state for clock, transmit data at the rising edge and sample input data at the end of data output time. Given f_{osc} = 16MHz. ***03***

4B. Describe the USB protocol for bulk transfer. Explain Token, data and handshake packets. ***04***

4C.

i. In case of on-chip ADC of PIC16F877 with reference voltages, V_{ref+} =4V and V_{ref-} = 0V, if analog input voltage is 3.7V, determine the digital output and hence the values of ADRESH and ADRESL registers with left justified result.
ii. Describe the algorithm for converting analog input to digital by on chip ADC in PIC 16F877 microcontroller.

03

5A.

i. Describe the features, working and timeout selection details of watchdog timer in PIC16F877 microcontroller.
ii. With the help of a relevant pseudocode, explain how ATM timeout can be realized using watchdog timer.

04

5B. Four peripherals, P1, P2, P3 and P4 are to be connected to a processor in daisy chain arbitration scheme. P1, P2 and P4 are daisy chain compatible while P3 is not daisy chain aware. Design and draw a suitable logic circuit to make P3 daisy chain compatible. Explain the working, considering a relevant example. ***03***

5C. List the various metrics to be optimized while designing an embedded system and describe in detail the time to market design metric. ***03***