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# MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

*(A constituent unit of MAHE, Manipal)*

**SEVENTH SEMESTER BTECH. (E & C) DEGREE END SEMESTER EXAMINATION**
**MARCH 2021**
**SUBJECT: ADVANCED EMBEDDED SYSTEM DESIGN (ECE - 4001)**

**TIME: 3 HOURS** **MAX. MARKS: 50**

**Instructions to candidates**

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Discuss in detail the services provided by the operating system.

1B. What is a process? Explain the process data structure. Write the difference between process and thread. Write how an operating system is useful in handling multiprocessing?

(5+5)

2A. Explain the kernel, types of kernel and kernel services.

2B. Explain the steps used in the project creation using RTX. Briefly explain RTX kernel.

2C. Show how to handle concurrent execution with the help of program. Which kernel object is used to handle the concurrent execution? Explain.

(4+3+3)

3A. Write a RTX code for LPC1768 to blink the LEDs for every second. Use os_itv_wait() function for the delay. Simultaneously display the message TASK X for each task, where X= 1, 2 respectively.

3B. Elaborate the uses of threads in a single-user multiprocessing system.

3C. Discuss the modes of operations of cortex M3 processor. Draw the state diagram of the operation mode transition for ARM Cortex M3.

(4+3+3)

4A. Describe the following features of Cortex M3 processor core: architecture, instruction set, instruction execution, pipe-line, major internal core blocks. What's new comparing to the ARM7 core?

4B. Define the various concurrency mechanisms used in the operating system. Demonstrate how Semaphore function can be used in RTX code for LPC1768 to increment and print the value of a global variable ‘N’ continuously.

(5+5)

5A. Write an RTX code for LPC1768 using an event function to multiply the 2 numbers in one task and display the product in another task by changing the priority.

5B. Explain the following scheduling algorithms: i. SPN ii. HRRN

5C. With a neat sketch explain the boundary scan architecture.

(4+3+3)