Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SEVENTH SEMESTER BTECH. (E & C) DEGREE END SEMESTER EXAMINATION
MARCH 2021
SUBJECT: RTL VERIFICATION USING VERILOG (ECE - 4021)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Consider the following scheduled graph as shown in **Fig. 1A**. Apply Clique partitioning algorithm and determine the operation binding resources for MUL and ALU.

1B. Draw ROBDD for 3-bit counter that counts in the sequence of 0, 1, 2, 5, 7, 0… if the select bit is 0 and if the select bit is 1 it counts in the sequence of 3, 4, 6, 3,…. Show all the steps. Apply ITE algorithm for BDD.

1C. Draw the control and data flow graph for 2 input XOR gate using 4:1 mux.

(4+3+3)

2A. Apply Hu Algorithm for the sequencing graph shown in **Fig. 1A**. Determine the minimum number of resources to complete entire schedule. Given P(0)=1, P(1)=3, P(2)=4, P(3)=2, P(4)=2, remaining P values if any, need to be assumed as 2. Draw the rescheduled graph.

2B. Write Vams code for RLC circuit to measure voltages across resistor, capacitor and inductor. The parameter values can be suitably assumed.

2C. Draw technology schematic for 2:1 multiplexer. Assume the interfaced device is Xilinx FPGA.

(4+3+3)

3A. Obtain the set of prime implicants for the Boolean expression using tabular method
$F(a, b, c, d)=\sum m(0, 1, 6, 7, 8, 9, 13, 14, 15)$

3B. Write a sequential VHDL code for negative edge triggered JK flip flop.

3C. Consider the sequencing graph in Fig:1, All the operations are having unit execution delay. Using ASAP unconstrained algorithm, determine the latency. Also calculate mobility using ALAP algorithm.

(4+3+3)

4A. Determine the essential prime implicants for the set of prime implicants for the given Boolean expression using ESPRESSO algorithm.
$F=\sum m(1, 2, 4, 8)$

4B. Draw OBDD for $F(a, b, c, d)=\sum m(0, 1, 5, 7, 8, 10, 14, 15)$ in the order of b, d, a, c.

4C. Write Vams code for the voltage follower circuit. The parameter values can be suitably assumed.

(4+3+3)

5A. Write the structural VHDL code for 4-bit parallel adder. Assume full adder as the component.

5B. Determine the prime implicants for the following Boolean expression using iterative consensus method. F=∑m(0, 2, 3, 4, 5, 6)

5C. Reduce the state diagram given in **Fig. 5C** using implicant chart table technique. Draw the reduced state diagram.

(4+3+3)

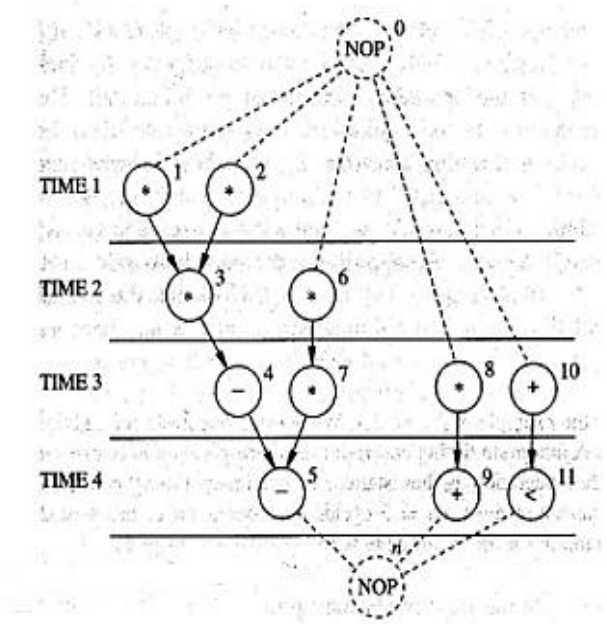

Fig. 1A

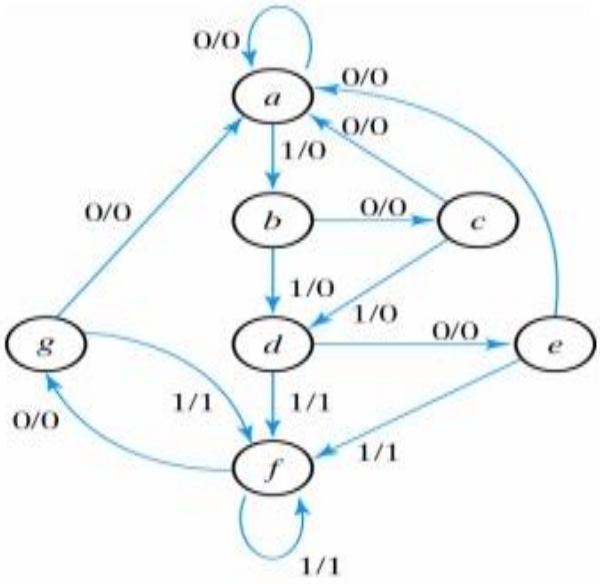

Fig. 5C