Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SEVENTH SEMESTER BTECH. (E & C) DEGREE END SEMESTER EXAMINATION
DECEMBER 2020/JANUARY 2021
SUBJECT: RTL VERIFICATION USING VERILOG (ECE - 4021)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Consider the sequencing graph given in **Fig. 1A**. Assume the execution delays of the multiplier and the ALU are 2 and 1 cycle respectively. Calculate mobility using ALAP algorithm. Also determine the number of resources using Hu algorithm. Assume P(0)=1; P(1)=3; P(2)=4; P(3)=2; P(4)=2. If any other P values exists, it needs to be assumed as 2. Draw the rescheduled graph.

1B. Draw the control and data flow graph for F = (A XOR B) + (C XOR D)

1C. Define the term RTL schematic and technology schematic

(4+3+3)

2A. Draw the sequencing graph for F=Y – [[[(A*B)*(L*M)*C]*D]*R] < (P+Q)] – [R–S]. Apply Clique partitioning algorithm and determine the operation binding resources for MUL and ALU. Show all the steps. Assume only two input operations are available in the sequencing graph.

2B. Find out the prime implicants for the following expression using Iterative consensus method F= $X'Z' + XYZ' + XY'Z' + XY'Z$

2C. Draw ROBDD for F=AB+BC+CA. Show all the steps starting from BDD.

(4+3+3)

3A. Apply LIST-L Scheduling algorithm for the given data flow graph shown in **Fig.1A**. Assume γ=4, $M_1=M_2=M_3=M_4=M_5=0$; $M_6=M_7=1$; $M_8=M_9=M_{10}=M_{11}=2$. Draw the scheduled graph under resource constraints.

3B. Write the behavioural VHDL code for 8:3 priority encoder. Use STD_MATCH function.

3C. Write the syntax for electrical and parameter declaration in Verilog AMS.

(4+3+3)

4A. Find the essential prime implicant for the set of prime implicants F={C_1, C_2, C_3, C_4} where $C_1=X2X3'X4'$, $C_2=X3X4$, $C_3=X1X2$, $C_4= X1'X3'X4'$ using ESPRESSO algorithm.

4B. Write the Verilog AMS code for the given expression to calculate $I = C.dv/dt$ Use parameter declaration. The values can be suitably assumed.

4C. Define the term two level minimization and explain its types.

(4+3+3)

5A. Write a sequential VHDL code for the given state diagram shown in **Fig. 5A.**

5B. Draw ROBDD for 3 bit synchronous prime number counter. Show all the steps starting from BDD. Perform ITE algorithm for BDD.

5C. Explain the flow of Digital VLSI design and verification.

(4+3+3)

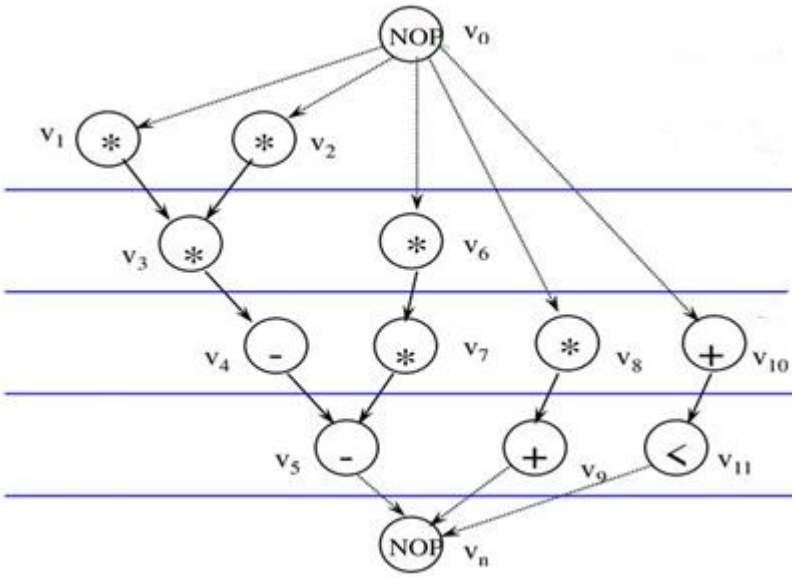

Fig. 1A

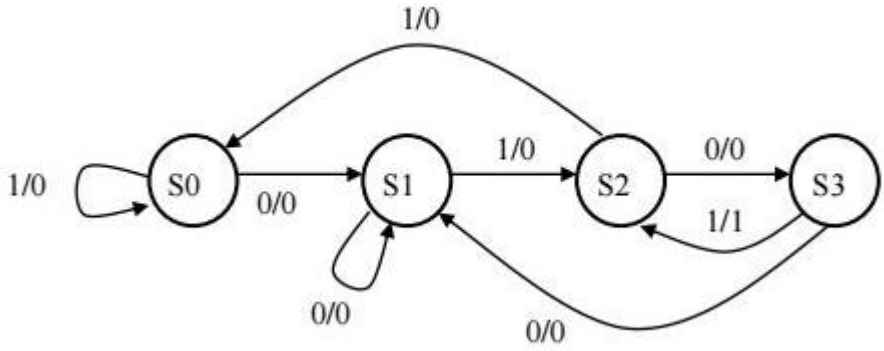

Fig. 5A