Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

VII SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)
ONLINE EXAMINATIONS, JANUARY – FEBRUARY 2021

EMBEDDED PROCESSOR ARCHITECTURE [ELE 4003]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 29 January 2021** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Processor can execute two instructions at a time, Load (LD) and Store (ST) have 2 cycle latencies and all other instructions have 1 cycle latencies

```
ADD R2, R2, R3
LD R4,[R5]
SUB R7,R1,R9
MUL R5,R4,R4
SUB R1,R12,R10
ST [R13],R14
OR R15,R14,R12
```

a) Write the optimal flow of execution.
b) Calculate the CPI for before and after the optimal flow. ***(04)***

1B. Processor is designed 5 instructions and 5-stage pipeline as shown in the Figure1. 30ps is the latency added due to buffer registers in between the stages. Calculate total time taken and throughput of pipeline .

IF	ID	EX	MEM	WB
210ps	90ps	110ps	240ps	50ps

Figure 1 ***(03)***

1C. Explain the different methods to eliminate the Structure Hazards in pipeline. ***(03)***

2A. List out the features of Instruction Set Architecture (ISA) of Typical RISC Processors. ***(04)***

2B. With the neat diagram and examples (instructions), Summarize the use of Barrel Shifter in ARM data flow model. ***(03)***

2B. With the example explain the significance of Multiple Register transfer implemented in ARM Architecture. ***(03)***

3A. Outline the various function of CP15 registers implemented in ARM 920T. ***(05)***

3B. With neat diagram of CP15-C1 register, explain the significance of bits in controlling the system parameters of ARM 9ES. ***(05)***

4A. Explain the significance Tightly coupled memory (TCM) and how it is implemented in ARM 946E-S. ***(05)***

4B. List out the various functions and instructions of Cache operation register C7 of CP15 register. ***(05)***

5A. Explain, How split transaction and pipelined transfer is implemented in AMBA Bus Architecture. ***(05)***

5B. With neat diagram, explain the Advanced High Performance Bus (AHB) interconnection. ***(05)***