Reg. No. | | | | | | | | | | |

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SEVENTH SEMESTER B.TECH. (INSTRUMENTATION AND CONTROL ENGG.)

END SEMESTER DEGREE EXAMINATIONS, JANUARY - 2021

SUBJECT: VLSI DESIGN [ICE 4001]

03-02-2021

TIME: 3 HOURS MAX. MARKS: 50

Instructions to candidates :*Answer ALL questions and missing data may be suitably assumed.*

1A. Compare various VLSI technologies based on their speed to power performance.

1B. What are enhancement mode and depletion mode transistors? Explain differences based on their mechanism of operation.

1C. With neat diagrams explain the p-well process for CMOS fabrication.

(2+3+5)

2A. What are the building blocks of an FPGA?

2B. Explain body effect.

2C. Obtain the pull-up to pull-down ratio for an nMOS inverter driven through four pass transistors.

(2+3+5)

3A. Write a note on the limits of miniaturization.

3B. Design a 4:1 multiplexer in CMOS logic.

3C. Prove that the changeover between logic levels is symmetric for a CMOS Inverter.

(2+4+4)

4A. How do the static and dynamic components of power dissipation contribute to scaling factor?

4B Calculate the capacitance for Metal 1(L = 16λ, W = 3λ) shown in fig Q4B. How will the capacitance be if the area of same material is i) polysilicon, ii) n-type diffusion.

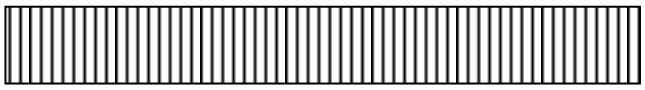

Fig. Q 4B

4C Draw a 2 Input XOR gate in CMOS logic and represent it in stick notation.

(2+3+5)

5A. Differentiate between semicustom and full custom IC design.

5B. Model the relationship between built in junction potential and the applied voltage.

5C. With a neat diagram explain the configuration of Boundary Scan test.

(2+4+4)