Reg. No. | | | | | | | | | |

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SEVENTH SEMESTER B.TECH. (INSTRUMENTATION AND CONTROL ENGG.)

END SEMESTER DEGREE EXAMINATION, MARCH - 2021

VLSI DESIGN [ICE4004]

TIME: 3 HOURS 26-03-2021 MAX. MARKS: 50

Instructions to candidates :*Answer ALL questions and missing data may be suitably assumed.*

1A. Compare CMOS and BiCMOS technologies.

1B. With neat diagrams illustrate the steps involved in a typical n-well process.

1C. Explain enhancement mode transistor action for various drain voltages.

(2+4+4)

2A. Derive the expression for transconductance g_m of transistor.

2B. Describe different aspects of the MOS transistor threshold voltage V_T.

2C. Explain the working of an NMOS inverter and obtain the pull-up to pull-down ratio for an NMOS inverter driven by another NMOS inverter.

(2+4+4)

3A. What is the standard unit of capacitance? Specify its significance.

3B. Prove that the delay over a pair of cascaded NMOS inverters is constant.

3C. Design a 2 input NAND gate in CMOS logic and represent the same in stick notation.

(2+3+5)

4A. Explain two principles of CMOS design that enhance design process?

4B Obtain the pull-up to pull-down ratio for an inverter driven by pseudo-NMOS logic.

4C Prove that the changeover between logic levels in a CMOS inverter is symmetrically disposed about the point at which $V_{in} = V_{out} = 0.5\ V_{DD}$

(2+3+5)

5A. Discuss briefly the importance of DRCs?

5B. Explain signature analysis in BIST.

5C. With neat diagrams, explain various FPGA architectures.

(2+3+5)

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