INTERNATIONAL CENTRE FOR APPLIED SCIENCES
MAHE, MANIPAL
B.Sc. (Applied Sciences) in Engg.
End – Semester Theory Examinations – May 2021- Repeaters 2018 Batch
II SEMESTER- COMPUTER ORGANIZATION AND ARCHITECTURE (ICS 122)
(BRANCH: CSE)

Time: 3 Hours **Date: 22 May 2021** **Max. Marks: 100**

- ✓ **Answer ANY FIVE full Questions.**
- ✓ **Missing data, if any, may be suitably assume.**

1A Explain the Different Types of modern computers. (8)

1B Draw the flow chart for Booths algorithm and Multiply 4 x -6 using this algorithm. (6)

1C How do you represent a binary floating point number? Add the floating point numbers +9.75 and +18.5625. (6)

2A Explain the following addressing modes with example. (8)

i. Absolute
ii. Indirection and Pointers
iii. Indexing and Arrays
iv. Relative Addressing

2B For all the possible 3-bit binary patterns, tabulate the decimal equivalents in sign and magnitude, 1s complement and 2s complement systems. (4)

2C
i. Write a RISC-style program for adding 'N' elements of two vectors 'X' and 'Y' and storing the results in another vector 'Z'. Assume that the memory is byte-addressable and 1 word = 8 bytes. (8)
ii. Write a CISC-style program for the above problem.

3A With neat diagram Instruction Cycle State Diagram. (8)

3B Write and explain micro operations for fetch cycle (instruction fetch) by making use of data flow diagram and sequence of events. (8)

3C Construct a 1.5M x 64 larger memory using 256K x 16 smaller memory chips. (4)

4A Draw and Explain the Block Diagram of the Control Unit. (7)

4B With neat diagram explain single address field sequencing techniques in the case of micro instruction (6)

4C Draw and explain Wilkes's Micro Programmed Control Unit. (7)

5A Draw the internal organization of a 16 x 8 memory chip. Clearly indicate the data, address and control lines. Also, calculate the number of external connections. (6)

5B Explain the virtual memory address translation process with a neat diagram. Describe TLB. (7)

5C How can cache performance be enhanced by prefetching and lockup-free cache. Discuss. (7)

6A Draw the flowchart for unsigned binary division. Using this flowchart, divide 7 by 3. (8)

6B Explain in brief an I/O interface with a neat diagram. (4)

6C Discuss the input data transfer using the handshake protocol with a neat timing diagram. List the advantages and disadvantages of asynchronous bus. (8)

7A State why interrupt-enable and interrupt-disable are needed? How are they achieved? Explain vectored interrupts. (6)

7B Differentiate a parallel port from serial port. Explain printer to processor connection using a parallel port with a neat sketch. (6)

7C Discuss the following: (8)

(i) Branch delay slot in pipelining with an example.

(ii) Ideal case of pipelining with an example.

8A Write the syntax and description for the vector instructions VectorAdd, VectorLoad, and VectorStore. (6)

8B Consider the following C language loop to add vector elements: (6)

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for(i=0;i<N;i++)
 C[i]=A[i] + B[i];
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Write the vectorized form of the loop.

8C Discuss the graphical processing units. (8)

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