INTERNATIONAL CENTRE FOR APPLIED SCIENCES
MAHE, MANIPAL
B.Sc. (Applied Sciences) in Engg.
End – Semester Theory Examinations – May 2021
II SEMESTER- COMPUTER ORGANIZATION AND ARCHITECTURE (ICS 122)
(BRANCH: CSE)

Time: 3 Hours **Date: 22 May 2021** **Max. Marks: 50**

- ✓ **Answer ALL Questions.**
- ✓ **Missing data, if any, may be suitably assume.**

1A Draw the block diagram of Basic functional units of a computer. Explain the types of memory unit and ALU. (6)

1B Draw the flow chart for Booths algorithm and Multiply 5 x -6 using this algorithm. (4)

2A Represent the following in 32-bit IEEE floating point format. (4)

i. 23.5
ii. 2.6875

2B Explain register organization. (6)

3A With neat diagram explain two address field sequencing technique in the case of micro instructions. (5)

3B Answer the following: (5)

(i) Define hit rate, miss rate and miss penalty.
(ii) Write the formula for average access time experienced by the processor when there is only one level of cache.
(iii) Repeat (ii) when there are two levels of cache.

4A A cache consists of a total of 64 blocks, each of which accommodates 32 words. The main memory comprises 2048 blocks, each consisting of 32 words. (4)

(i) How many bits are there in main memory address?
(ii) How many bits are there in each of the fields of the main memory address, if direct mapping is used?
(iii) How many bits are there in each of the fields of the main memory address, if set-associative mapping (each set has 4 blocks) is used?

4B Define an interrupt. Explain how an interrupt request is handled by the processor with the help of a neat diagram. How can interrupt latency be reduced? (6)

5A With an example, explain how unconditional branches cause instruction hazards. Also, state how the stall can be reduced in such cases. (4)

5B Discuss how cache coherence is achieved in shared memory multiprocessor systems by write-through and write-back protocols. Also, compare and contrast these protocols. (6)

****