INTERNATIONAL CENTRE FOR APPLIED SCIENCES
MAHE, MANIPAL

B.Sc. (Applied Sciences) in Engg.

End – Semester Theory Examinations – May 2021

II SEMESTER: LOGIC DESIGN (IEC 121)
(BRANCH: E & E)

Time: 3 Hours **Date:22 May 2021** **Max. Marks: 50**

- ✓ **Answer ALL Questions.**
- ✓ **Missing data, if any, may be suitably assume.**

1A. Design a 3-bit binary up-down counter. **(5)**

1B. Design a Full adder using 3:8 Decoder. **(5)**

2A. Implement the following switching functions using a Four input multiplexer F(A, B, C, D) = ∑m (0, 1, 2, 4, 6, 9, 10, 13, 14). **(5)**

2B. Reduce the Boolean function f (w, x, y,z)= ∑m (0,1,4,8,9,10) with don't cares condition d (w, x, y, z)= ∑ m (2,11) using k-map technique and implement using gates. **(5)**

3A. Perform 2's complement subtraction of 010110-100101 **(2.5)**

3B. Convert $(53)_{10}$ to EX-3 code. **(2.5)**

3C. Why digital circuits are more frequently constructed with NAND or NOR gates than with AND & OR gates? Explain. **(2.5)**

3D. Convert 110011 into hexadecimal through octal. **(2.5)**

4A. Design a sequence generator for the following sequence "1011". Show all the required steps. Assume overlapping is allowed. **(5)**

4B. Construct and explain a Ring counter for five timing signals. **(5)**

5A. Design 16:1 MUX using only 2:1 MUX . **(5)**

5B. Explain with logic diagram the operation of 4-bit SIPO unidirectional shift register. **(5)**

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