INTERNATIONAL CENTRE FOR APPLIED SCIENCES
MAHE, MANIPAL
B.Sc. (Applied Sciences) in Engg.
End – Semester Theory Examinations – May 2021
IV SEMESTER- DSD USING VERILOG (IEC-244)
(BRANCH: E & E)

Time: 3 Hours **Date: 19 May 2021** **Max. Marks: 50**

- ✓ **Answer ALL Questions.**
- ✓ **Missing data, if any, may be suitably assumed.**

1A. Map the function F(a,b,c,d)=abc+ab'c+ cd' using Xilinx XC 3000 FPGA. Determine the number of CLB's and LUT's required. Show the contents in the SRAM cell. **(5)**

1B. Compare full custom and semicustom ASIC with examples. **(5)**

2A. Implement the following function F=A'B+ABC'+A'B'C using ACT 1 logic module. **(5)**

2B. Consider the circuit takes two inputs A and B of 2bit width (i.e A1 A0 and B1 B0) Write the truth table for the circuit which gives logic high output when the inputs are equal else '0'. Implement the same using ALTERA with 4 x 3 x 3 **(5)**

3A. Find the essential test vector and selective test vector for the function F=A'B+C using fault table technique. Consider SA0 at B and SA1 fault at C. **(5)**

3B. Write a Structural Verilog code for 8:1 multiplexer using 2:1 multiplexer. Write the program for entire hierarchy. **(5)**

4A. Find the test vector using path sensitization technique for the expression F=(A.B)'+(C.D)'. Consider SA_0 fault is at input A node. **(5)**

4B Write the behavioral Verilog code for 4 bit SISO shift register using if statement. **(5)**

5A. Write a dataflow Verilog code for 2to 4 decoder with active high enable input. **(4)**

5B. Explain following interconnects with neat diagram
a. Antifuse b. SRAM c. EEPROM **(6)**

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