INTERNATIONAL CENTRE FOR APPLIED SCIENCES
MAHE, MANIPAL
B.Sc. (Applied Sciences) in Engg.
End – Semester Theory Examinations – May 2021
IV SEMESTER- VLSI DESIGN (IEC 243)
(BRANCH: E & E)

Time: 3 Hours **Date: 17 May 2021** **Max. Marks: 50**

- ✓ **Answer ALL Questions.**
- ✓ **Layout must be drawn using the graph sheet provided**.
- ✓ **Missing data, if any, may be suitably assumed.**

1A. i) Define figure of merit. What is the significance of figure of merit?

ii) Derive the expression for MOS transistor transconductance g_m and output conductance g_{ds}. **(5)**

1B. The MOSFET in **Figure 1B** has V_t= 1V and $\mu_n Cox(W/L)$ = 1 mA/V^2 . Find the drain current and drain voltage for V_G = 2V and R_D = 1k**Ω**. **(5)**

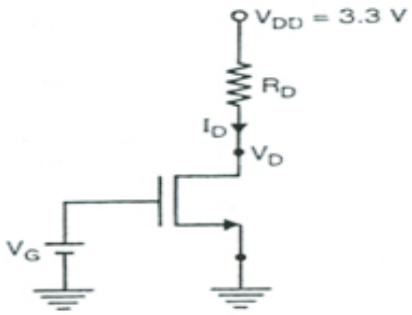

Figure 1B

2A. Define latch-up in CMOS. Why does it occur? What are the remedies for latch- up? Explain in detail with necessary circuit diagrams and curve. **(5)**

2B. Derive the required ratio between Zp.u. and Zp.d. if an NMOS inverter with depletion mode pull up is to be driven from another NMOS inverter with depletion mode pull up . **(5)**

3A. An engineer from FAIRCHILD SEMICONDUCTOR is experiencing the leakage current due to latch-up in standard CMOS IC. While searching for the solutions, he stumbles upon a set of files where a possible solution to leakage problem is addressed. These files contain following information

(i) Silicon is epitaxially grown on sapphire or magnesium aluminate spinel.
(ii) All the layers are grown onto the substrate.
(iii) PMOS and NMOS transistor are fabricated into small island onto the substrate. Density of transistors are very high.
(iv) No problem of field inversions exits.

Identify the type of MOS fabrication and explain the complete fabrication process with neat diagram. **(5)**

3B. Draw the circuit, stick diagram and layout of two input NAND gate using CMOS design style. **(5)**

4A. Give the circuit implementation of following multiple output functions using NMOS based PLA. Give the stick notation. $Z_1 = AB + \bar{A}\bar{B}C$; $Z_2 = AB$; $Z_3 = A + \bar{B}C$, $Z_4 = ABC + \bar{B}\bar{C}$ **(5)**

4B. Consider a CMOS inverter with the following device parameters shown in Table 4B.

Table 4B

parameter	NMOS	PMOS
μC_{ox}	$60\ \mu A/V^2$	$20\ \mu A/V^2$
V_{th}	0.6 V	- 0.8 V
$V_{dd} = 3\ V, V_{ss} = 0\ V$		

Determine the ratio of $\frac{L_n/W_n}{L_p/W_p}$. Given, the switching threshold voltage 1.5 V. **(5)**

5A. State and explain the three different scaling models. Discuss the effect of scaling using Combined V and D, Constant E and Constant V models on following parameters: [i] Gate area A_g [ii] Gate capacitance per unit area C_o [iii] Carrier density in channel Q_{on} [iv] Maximum operating frequency f_o. **(5)**

5B. Derive the expression for rise time estimation and fall time estimation of CMOS inverter. What are the significance of rise time and fall time? **(5)**