Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

III SEMESTER B.TECH.(COMPUTER AND COMMNUNICATION ENGG)
MAKEUP/GRADE IMPROVEMENT EXAMINATIONS, JULY 2021

SUBJECT: DIGITAL SYSTEMS AND COMPUTER ORGANIZATION

[ICT 2171]

REVISED CREDIT SYSTEM
(23/07/2021)

Time: 2 Hours MAX. MARKS: 40

Instructions to Candidates:

- Answer **ANY FOUR FULL** questions.
- Missing data may be suitably assumed.

1A. Design a single digit BCD adder/subtractor in which the inputs are in excess-3 code, using 7483 ICs and logic gates. **6**

1B. Design a 1 – bit magnitude comparator with cascading inputs using NAND gates ONLY. Using the same as a block, design a 3 – bit magnitude comparator. **4**

2A. Design a 3-bit binary to gray code converter using minimum number of 74153 ICs ONLY. **6**

2B. Design a combinational circuit using 74138 IC that takes (7 5 3 -6) code as 4-bit input and generates an output high if the input is in the range 0 to 3. Use a logic gate so as to minimize the total number of input terminals. **4**

3A. Design MOD 14 asynchronous counter using
i. 7493 ICs and minimum external gates to generate output with 50% duty cycle.
ii. 7490 ICs and external gates. **6**

3B. Design a 2 – bit synchronous UP/Down counter using negative edge triggered T – flip flops and external gates. **4**

4A. Using 74193 ICs, 7485 ICs and external gates, design a 2 – digit decimal DOWN counter which counts from N1 to N2 and repeats. **6**

4B. Design a sequence generator circuit to generate the sequence 1101000 using asynchronous down counter. Use negative edge triggered D – Flip flops and minimum external gates for the design. **4**

5A. Design a sequence detector circuit with one input Y and one output Z. The output Z is HIGH whenever the sequence "1001" is detected, otherwise the output is LOW. Overlapping of the sequence is allowed. Implement using JK - flip flops and minimum number of external gates. **6**

5B. Explain the general purpose microprogrammed control unit design. How is it different from hardwired design approach? **4**

6A. Why is non-restoring division algorithm preferred over restoring division algorithm? Perform the division of $(13)_{10}$ by $(6)_{10}$ using the non-restoring division algorithm indicating all the steps. **6**

6B. How does a set associative cache mapping technique overcome the limitations of fully associative and direct mapping techniques? Explain with respect to a computer system that has a 24K of main memory and 2K of cache memory. Cache memory block is 8 words. Assume 2 blocks/set. **4**