Question Paper

Exam Date & Time: 03-Mar-2021 (09:00 AM - 12:00 PM)

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

THIRD SEMESTER B.TECH END SEMESTER EXAMINATIONS, MARCH 2021

DIGITAL SYSTEMS AND COMPUTER ORGANIZATION [ICT 2171]

Marks: 50 **Duration: 180 mins.**

A

Answer all the questions.

1)		Design a 3 - bit binary Carry Look Ahead (CLA) adder circuit using logic gates. If the propagation delay of logic gate is 't', what is the time required to add two, 6 - bit binary numbers using CLA? Justify.	(5)
	A)		
	B)	Design a sequence detector circuit with one input Y and one output Z. The output Z is HIGH whenever the sequence "101" is detected, otherwise the output is LOW. Overlapping of the sequence is allowed. Implement using T - flip flops and minimum number of external gates.	(3)
	C)	Design a 3-bit magnitude comparator using 7483 IC and NOR gates ONLY.	(2)
2)		Design a code converter to convert a decimal digit represented in excess -3 code to a decimal digit represented in gray code, using 74138 ICs and external gates.	(5)
	A)		
	B)	Design JK - flip flop using NAND latch and external gates.	(3)
	C)	Explain the concept of carry save adder with the help of an example.	(2)
3)		Design a microprogrammed control unit for 4 - bit x 4 - bit Booth's multiplier.	(5)
	A)		
	B)	Design a 4 - bit asynchronous presettable Down counter to count from $(1100)_2$ to $(0110)_2$ using negative edge triggered D - flip flops and external gates.	(3)
	C)	Explain daisy chain technique to handle multiple interrupts with the help of neat diagram.	(2)
4)		Using 74193 ICs, 7485 ICs and external gates, design a 2 - digit decimal UP counter which counts from N1 to N2 and repeats.	(5)
	A)		
	B)	A Computer system has a 64K blocks of main memory and 8K blocks of cache memory. The block size is 8 words. Calculate the tag field width for fully associative mapping, direct mapping and 4-way set associative mapping schemes.	(3)
	C)	Design a sequence generator circuit to generate the sequence 10111001 using Johnson counter. Use D - Flip flops and minimum external gates for the design.	(2)
5)		Draw the flowchart of Non restoring division algorithm. Perform the division of $(12)_{10}$ by $(5)_{10}$ using the same algorithm indicating all the steps.	(5)
	A)		
	B)	Design full adder/ subtractor using minimum 4:1 Multiplexers and ONLY XOR gates.	(3)

C) Using ONLY 7490 ICs, design a MOD 10 counter circuit to generate an output waveform with 50% duty cycle. (2)

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