Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent institution of MAHE, Manipal)

III SEMESTER B.TECH. (COMPUTER SCIENCE AND ENGINEERING)

END SEMESTER EXAMINATIONS, MARCH 2021

SUBJECT: COMPUTER ORGANIZATION AND ARCHITECURE [CSE 2151]

REVISED CREDIT SYSTEM

(01/03/2021)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.

1A. With the help of a neat flowchart, explain the unsigned multiplication algorithm. Using that algorithm multiply the decimal numbers 54 (multiplicand) and 10(multiplier). Show the sequence of steps clearly and indicate the result. Use minimum number of bits required. **5**

1B. List two characteristics of RISC. Write a RISC style program to find the length of the string, if the string is terminated by '$' character. Assume that the string is stored starting from memory location named STRING and store the length in memory location LENGTH. **3**

1C. Explain big endian and little endian assignments. Show how the value 12345678 is stored in memory starting from word address 8000 in both big endian and little endian assignments, if the word comprises of 16 bits. **2**

2A. For the Register Transfer Description Algorithm given below,

```
Declare Registers A[8], B[8], C[8];
START:  A←0;
        B←00001010;
LOOP:   A←A+B;
        B←B-1;
        If B<> 0 then goto LOOP;
        C←A;
HALT:   GO to HALT;
```

(i) Draw the processing section for implementing the algorithm, identifying all the control points. Also list the control points and the operations performed.

(ii) Draw the state diagram. Indicate the operations performed and the control signals activated in each state **5**

(iii) Write the truth table of sequence controller and draw the PLA diagram.

2B. Represent 0.25 and +5.25 using 32 bit IEEE floating point representation. Add the two numbers using the rules for addition of floating point representation and show the result in 32 bit IEEE floating point representation. Indicate clearly all the steps **3**

2C. Identify the addressing modes in each of the following instructions and explain the same.

(i) Add R2, R1, R3
(ii) Load R1, LOC
(iii) Move R1, #LOC
(iv) Move R2, (R3) **2**

3A. (i)Explain single bus, and two bus oriented ALU with necessary diagrams. Which one is advantageous with reference to speed of operation? Justify your answer **3**

(ii)The control signals C0 to C10 are grouped into three groups as given below **2**

Group 1: C0, C4, C5, C8, C9
Group 2: C1, C10, C7
Group 3: C2, C3, C6

Draw the diagram showing how the control signals are encoded in partially encoded format

3B. With an example, explain how unconditional branches cause instruction hazards. Also, state how the stall can be reduced in such cases. **3**

3C. The processor's waiting time gets reduced with Early-restart protocol in memory system. Give a detailed justification to this statement. **2**

4A. Discuss how cache coherence is achieved in shared memory multiprocessor systems by write-through and write-back protocols. Also, compare and contrast these protocols. **5**

4B. Define DMA transfer. Mention clearly, the role of processor in a DMA transfer. With a neat sketch, explain the registers of DMA controller and how they are used during a DMA transfer **3**

4C. Consider the following instructions:

```
Add R3, R2, #20
Subtract R5, R4, #3
And R6, R4, #0x3A
Add R7, R2, R4
```

These instructions are executed in a computer that has a five-stage pipeline (Fetch, decode, compute, memory and write). The first instruction is fetched in clock cycle 1, and the remaining instructions are fetched in successive cycles. Draw a diagram that represents the flow of the instructions through the pipeline. **2**

5A. A 3 × 5 array of numbers, each occupying one byte, is stored in main memory locations 5000 through 500E (hex). The elements of this array, A, are stored in row major order. Assume that each block in memory consists of only one 8-bit of data and the memory is byte-addressable with 16-bit addresses. The data cache has space for only eight blocks of data. Assume that the LRU replacement algorithm is used for block replacement in the cache. It is required to examine the changes in the data cache entries caused by running the following code. **5**

```
SUM=0;
for (j = 4; j >= 0; j-- )
   SUM = SUM + A(0, j);
AVG = SUM / 5;
for (i = 0; i < 5; i++ )
   A(0, i) = A(0, i) / AVG;
```

Show how these elements of the array A are stored in main memory. Show the contents of the cache change after various passes through the two loops in the above code using direct-mapped data cache and associative mapped cache. Also calculate the hit ratio of each of these mapping techniques.

5B. Prepare a table having the columns as '*number of sets*', '*number of blocks per set*', '*number of bits in set field of memory address*' for a k-way set associative cache with 256 blocks in the cache. Fill all the entries in the table you prepared for different number of blocks per set as 1, 2, 4, 8, 16, 32, 64, 128, 256. **3**

5C. Discuss the importance of control bits in Cache memory **2**