Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

III SEMESTER B.TECH. (COMPUTER SCIENCE AND ENGINEERING)

END SEMESTER EXAMINATIONS, NOVEMBER 2020

SUBJECT: DIGITAL SYSTEM DESIGN [CSE 2153]

REVISED CREDIT SYSTEM
(03/03/2021)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Draw the diagram for 3-bit array multiplier using full adders and half adders. Write the Verilog code for the same using half adder and full adder modules. Assume the inputs to the multiplier as A[2:0] and B[2:0] and the output as P[5:0]. **5M**

1B. Define Noise Margin. Write down the equations for low noise margin and high noise margin in logic circuits. Clearly mention the terms present in the equations. Also explain the type of power dissipation in logic circuits. **3M**

1C. Explain the CMOS realization of a NAND gate with the aid of truth table and circuit diagram. **2M**

2A. A sequential circuit has three T flip-flops, *A, B* and *C* and one input *x*. It is described by the following flip-flop input functions:

$$TA = (BC' + B'C)x + (BC + B'C')x'$$
$$TB = A$$
$$TC = B$$

i) Derive the state table for the circuit.
ii) Draw the state diagrams when x=0 and x=1 separately **(3+2)M**

2B Taking a, b and d as select signals, implement f(a,b,c,d)=Σm(1,2,5,8,10,13,14,15) using appropriate multiplexer and other necessary gates. **3M**

2C. Simplify the following expression using K-map. Write all the essential prime implicants and find the minimum cost SOP expression **2M**

$F(a,b,c,d) = \sum m(1,3,4,5,7,8,9,11,12,15)$

3A. Write the algorithm for bit counting circuit and draw its ASM chart. With respect to this, differentiate traditional flow chart and ASM chart. Also design the datapath circuit for the same and draw the ASM chart for its control circuitry. **5M**

3B. Explain the elements of ASM chart with their symbols. **3M**

3C. Draw the 3-bit Johnson counter. Write the count sequence and decoding logic required for the output. **2M**

4A. Derive the Flip Flop (FF) input equations for a synchronous BCD down counter using JK FFs. **5M**

4B. Derive the sequential circuit output and Flip Flop input equations that realize the FSM defined by the state-assigned table shown in Table Q4B. using SR Flip-Flops.

Table Q4B.

Present state y_2y_1	Next state $w = 0$ Y_2Y_1	Next state $w = 1$ Y_2Y_1	Output z
0 0	1 0	1 1	0
0 1	0 1	0 0	0
1 0	1 1	0 0	0
1 1	1 0	0 1	1

3M

4C. Distinguish between the following:

i) Synchronous and asynchronous clear

ii) Blocking and non-blocking assignments. **2M**

5A. Write the truth table for full adder and implement it using

i) Only 2:1 multiplexers and NOT gates

ii) 2:4 decoders and other necessary gates **5M**

5B. Draw the state diagram and write the state table for swapping the contents of two registers R1 and R2 in response to an input signal w. Use a temporary register R3. Initially the registers R1 and R2 are loaded with two different data in two different clock cycles. Explain the operations performed in different states. Also write the Verilog code snippet to define the next state combinational circuit for this FSM. **3M**

5C Use Shannon's expansion to implement f(c,b,a) = πM(0,4,5,6) using only 2:1 multiplexers. **2M**