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# MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
*(A constituent unit of MAHE, Manipal)*

## III SEMESTER B. TECH (ELECTRICAL & ELECTRONICS ENGINEERING)
## GRADE IMPROVEMENT / MAKEUP EXAMINATIONS, JULY/AUGUST 2021

## DIGITAL SYSTEM DESIGN [ELE 2152]

REVISED CREDIT SYSTEM

**Time: 2 Hours** **Date: 26 July 2021** **Max. Marks: 40**

**Instructions to Candidates:**

- Answer **any four complete questions**.
- Missing data may be suitably assumed/Mention the assumptions

**1A.** Design a 3 input, one output minimal two-level gate combinational network that has a logic 1 output when the majority of its inputs are logic 1 and has a logic 0 output when the majority of its inputs are logic 0.

a. using AND -OR realization method
b. using NAND-NAND realization method ***(05)***

**1B.** Simplify the expression F (a, b, c, d) using Quine Mc-Cluskey approach.

$$F(a,b,c,d) = \sum m\,(6,7,9,10,13) + d(1,4,5,11,15)$$ ***(05)***

**2A** Using 4-bit binary adder, design a single digit decade BCD adder circuit. ***(05)***

**2B.** Design a magnitude comparator circuit which compares two numbers A and B, each with 2 bits. Implement it using dual 4 to 1 multiplexer (input residual gates may be used, use A as select lines and B as data lines) ***(05)***

**3A.** Design a presettable counter which can count the states 9,10 ,11,12,13,14,15 ,9, 10, ….. using

a) D flip-Flop
b) JK Flip-Flop ***(05)***

**3B.** Design a digital circuit which generates the pattern 1001-1100-0110-0011-……. Repeats

a) using universal shift register IC
b) using D flip flops ***(05)***

**4A.** A sequential circuit has an input w and an output z. The machine has to generate z=1 when the previous values of w were 1001 and 010; otherwise z=0. Overlapping input patterns are allowed. Draw a single state diagram of the mealy machine to detect the sequences. Implement the circuit using D flip flops. ***(05)***

**4B.** Design a synchronous counter to count the sequence 1-3-5-7-1-3- …… using JK flip-flop. ***(05)***

**5A.** Define

a. Czochralski crystal growth

b. Doping and Diffusion

c. Oxidation

d. Photolithography

e. Etching ,

in Silicon processing ***(05)***

**5B.** Draw the circuit diagram of three input NOR gate and three input OR gate using CMOS logic. ***(05)***

**6A.** Write the difference between dataflow modeling, and gate level modeling in Verilog HDL. Illustrate the difference with example. ***(05)***

**6B.** Show how the functions, **f1 (a, b, c) = $\bar{a}$b + abc; f2(a, b, c) = $\bar{b}\bar{c}$ + ac** , can be realized using Programmable Logic Array. ***(05)***