Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

THIRD SEMESTER BTECH. (E & C) DEGREE END SEMESTER EXAMINATION
MARCH 2021
SUBJECT: DIGITAL SYSTEM DESIGN USING VERILOG (ECE - 2153)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Design a circuit using K-map which converts 4-bit XS-3 code to its equivalent BCD code. Implement the minimum expression using NOR logic only.

1B. Design and implement a 4-bit shift register which performs operations as given in **Table 1B.**

1C. Write a Verilog code for divide-by-6 ripple counter using negative edge triggered JK flip flops.

(4+3+3)

2A. Implement the following functions using Xilinx FPGA

$$F_1 = \bar{A}BC + \bar{B}C + AB$$
$$F_2 = \bar{A}B + A\bar{B} + A\bar{C} + \bar{A}C$$
$$F = \overline{F_1 \oplus F_2}$$

Show the interconnection between various blocks. Specify the number of CLBs and LUTs required. Implement the design and give the content of each LUT.

2B. For the given Boolean function, determine a minimal sum using VEM technique, where *x*, *y* and *z* are the map variables.

$$f(A, B, x, y, z) = Ax\bar{y}\bar{z} + A\bar{x}\bar{y}z + Ax\bar{y}z + \bar{B}\bar{x}\bar{y}z + B\bar{x}y\bar{z} + \bar{x}yz + \bar{x}\bar{y}\bar{z}$$

2C. Implement 1010 overlapping sequence detector using Moore model. Use positive edge triggered D flip flop and required logic gates.

(4+3+3)

3A. Design a synchronous counter which goes through 0, 3,6,7 using positive edge triggered XY flip flop and all unused states will go to '0'. The truth table of XY flip-flop is given in **Table 3A.**

3B. Write a structural Verilog code for 2-bit comparator using 1-bit comparator and built-in primitives.

3C. Consider the circuit shown in **Fig. 3C**. Map the circuit using minimum number of decoder and basic gates.

(4+3+3)

4A. Consider the Boolean network given by the following equations

$$U_1 = U_2U_4U_5; \quad U_2 = U_3U_4; \quad U_3 = CU_4; \quad U_4 = A + D; \quad U_5 = BU_4;$$

where *A*, *B*, *C*, and *D* are PI's and U_2, U_3, U_4, and U_5 are intermediate I/O's. There is only one output (PO). Implement the same using 2:1 MUX/s only as interconnected structure.

4B. Analyze the sequential circuit shown in **Fig. 4B** and draw its state diagram.

4C. Write sequential Verilog code for synchronous modulo-8 Gray code counter.

(4+3+3)

5A. Given the state table of a sequential circuit as shown in **Table 5A**, implement it using minimum number of ACT-2 S and ACT-2 C Module.

5B. Given the following three Boolean equations, representing part of the control logic for an air conditioner. Implement it using optimized number of suitable DEMUX(s) and multi-input basic gates.

heater_on = (temp_low) · (auto_temp) + manual_heat

cooler_on = (temp_high) · (auto_temp) + manual_cool

fan_on = (heater_on + cooler_on) + manual_fan

5C. Write a sequential Verilog code for 4-bit ripple carry adder using 1-bit full adder as basic block.

(4+3+3)

Table: 1B

S1	S0	Operation
0	0	Parallel Load
0	1	Johnson Counter
1	0	Shift left
1	1	Memory

Table: 3A

X	Y	Q(n+1)
0	0	1
0	1	0
1	0	$Q(n)^l$
1	1	Q(n)

Table: 5A

PS		I/P	NS		O/P
y_1	y_2	X	Y_1	Y_2	Z
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	0	1	1

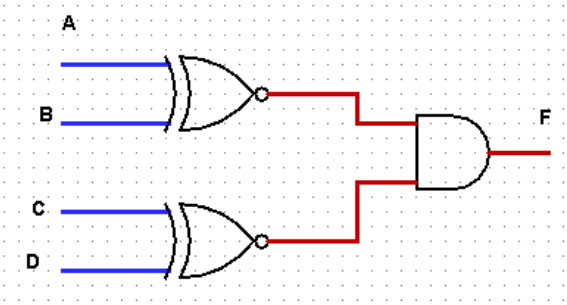

Fig. 3C

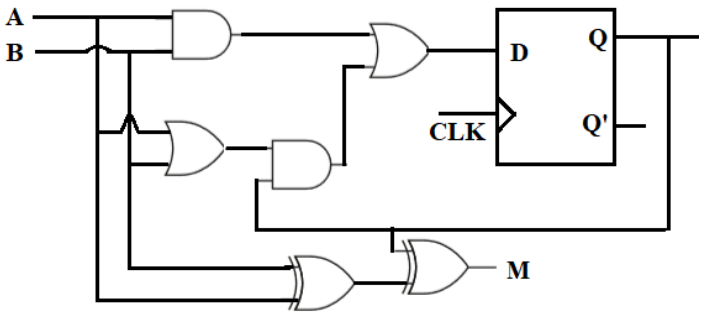

Fig. 4B