Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

DEPARTMENT OF MECHATRONICS ENGINEERING

III SEMESTER B.TECH. (MECHATRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, Month Year

SUBJECT: DIGITAL SYSTEM DESIGN [MTE 2152]

(Date)

Time: 3 Hours **MAX. MARKS: 50**

Instructions to Candidates:

- Answer **ALL** the questions.

Q. No		M	CO	PO	LO	BL
1A.	Design a combinational circuit which has four inputs A,B,C,D and three outputs X,Y,Z. XYZ represents a binary number whose value equals the number of 1's at the input.	**4**	**CO1**	**PO1 PO2 PO12**	**C1, C7, C13**	**3**
1B.	Implement full subtractor (x,y,B_{in} are inputs; d,B_{out} are outputs) using two 4 to 1 Multiplexers and residual gates, taking y and B_{in} as select lines.	**3**	**CO2**	**PO1 PO2 PO3 PO12**	**C2, C7, C9, C13**	**1,3**
1C.	Design a presettable counter which counts from 7 to 14, using D flip flops	**3**	**CO3**	**PO1 PO3 PO12**	**C3, C7, C8, C9, C13**	**3**
2A.	Implement the following expression using 3 to 8 decoders (Active high) and residual gates. $\mathbf{f(w,x,y,z) = \sum m(1,2,6,7,9,11,12,14)}$	**4**	**CO2**	**PO1 PO3 PO12**	**C2, C7, C9, C13**	**3**
2B.	Write a gate level Verilog code for a 1 bit full subtractor	**4**	**CO5**	**PO1 PO2 PO5 PO12**	**C6, C7, C8, C18**	**1,3**
2C.	Convert the given Hexadecimal number **F96AD** into its equivalent binary number. Hence obtain gray code of the same.	**2**	**CO2**	**PO1 PO2 PO12**	**C2, C7, C9, C13**	**1**
3A.	Implement a MOD 156 counter using 7493	**4**	**CO3**	**PO1 PO3**	**C3, C7,**	**3**

				PO12	**C8, C9, C13**	
3B.	What is race around condition? Mention the condition and type of flip flop in which it occurs. How can it be avoided?	**3**	**CO3**	**PO1 PO12**	**C3, C7, C8, C9, C13**	**1**
3C.	Write a data flow Verilog code for a 4 bit Full adder	**3**	**CO5**	**PO1 PO2 PO5 PO12**	**C6, C7, C8, C18**	**1, 3**
4A.	AB flipflop has a characteristic equation. $Q^+ = BQ + A\overline{Q}$ Construct AB flip flop using T Flip flop	**4**	**CO3**	**PO1 PO3 PO12**	**C3, C7, C8, C9, C13**	**3**
4B.	Briefly explain the following with block diagram 1. CPLD 2. FPGA	**4**	**CO4**	**PO1 PO6 PO12**	**C3, C7, C8, C13**	**1**
4C.	Using 74LS194 wired as a right shift register implement ring counter.	**2**	**CO3**	**PO1 PO3 PO12**	**C3, C7, C8, C9, C13**	**3**
5A.	Design a 3 bit binary down counter using D flip flops.	**4**	**CO3**	**PO1 PO3 PO12**	**C3, C7, C8, C9, C13**	**3**
5B.	Design a sequence detector (Mealy FSM) to detect the sequence 0110 in a continuous data input stream. Use T Flip flop.	**6**	**CO3**	**PO1 PO3 PO12**	**C3, C7, C8, C9, C13**	**3**