Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

FOURTH SEMESTER BTECH. (E & C) DEGREE END SEMESTER EXAMINATION
AUGUST 2021
SUBJECT: LINEAR INTEGRATED CIRUITS (ECE - 2253)

TIME: 2 HOURS **MAX. MARKS: 40**

Instructions to candidates
- Answer **any FOUR** full questions.
- Missing data may be suitably assumed.

1A. In the circuit shown in Fig. Q1A., the Op-amp is ideal.
   i. Determine v_N, v_P *and* v_0.
   ii. Determine the value of the resistance R that, if connected between the inverting input pin of the op-amp and ground, causes v_0 to double.

1B. In the circuit shown in Fig. Q1B(i), R_1 = 1kΩ, R=10kΩ and C=0.1μF, Slew Rate = 0.5V/μs and $\pm V_{SAT} = \pm 12V$. Determine and plot the output voltage for the input voltage and circuit details specified in Fig. Q1B(ii).

(5+5)

2A. In the circuit shown in Fig. Q2A, the Op-amps are ideal. Derive the expression for the output voltage v_0.

2B. In the circuit shown in Fig. Q2B., the Opamps are ideal.
   i. Determine the output voltage V_o.
   ii. Determine the current through R and R_F.

(5+5)

3A. In the filter circuit of Fig. Q3A, all resistors are 1kΩ and capacitors are 0.1μF. Determine the maximum and minimum values of cut-off frequency, Q and passband gain.

3B. Design a Butterworth filter circuit having the frequency response shown in Fig. Q3B(i). Use capacitance value of 0.1μF.

(5+5)

4A. In the circuit shown in Fig. Q4A, R_1 is varied from 0 to ∞. With V_{0sat} = ±12V, plot $|V_P|$ and ΔV_T as a function of R_1.

4B. In the circuit shown in Fig. Q4B, plot V_{01} and V_0 for the following cases. The output saturation voltage is ±12V.
   i) $R_1 = R_2 = R_3$ = 1kΩ and C = 0.1μF
   ii) R_1 = 1kΩ R_2 = 10kΩ, R_3 = 1kΩ and C = 1μF

(5+5)

5A. Design a 555 timer based astable multivibrator to generate the following outputs. Select C=0.1μF.
   i. Square wave signal of fixed frequency of 1KHz and 65%.duty cycle

ii. Square wave signal of frequency varying between 2KHz to 8KHz and fixed T_{ON} of 0.05msec

5B. For the circuit shown in Fig. Q5B determine the following:

i. Frequency of the output signal

ii. The variation in the output signal frequency, if V_C is varied between 5V and 7.5V.

(5+5)

6A. With the help of a block diagram and functional table, explain the operation of 8-bit successive approximation type ADC for converting an analog input of 5.655 volts to corresponding digital output. The full scale output is 10 volts.

6B. Design a binary weighted 5 bit DAC for the following specifications:
With only LSB set, DAC output should be - 0.3125V. Select V_{REF} =2V. What will be the full scale output voltage of the DAC.

(5+5)

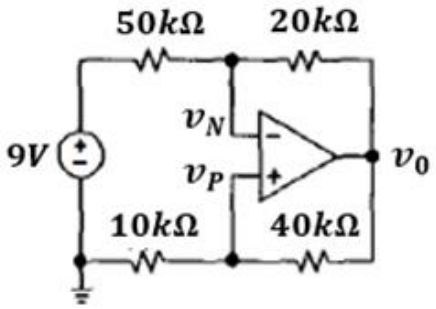

Fig. Q1A

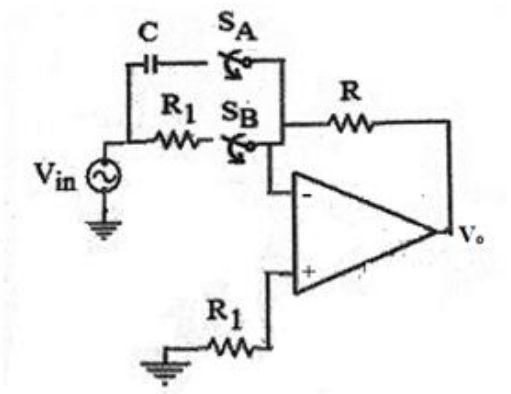

Fig. Q1B(i)

Sl. No.	V_{in} (Volts)	S_A	S_B
1	0.5sin2π1000t	Open	Closed
2	2sin2π20000t	Open	Closed
3	0.5sin2π1000t	Closed	Open

Fig. Q1B(ii)

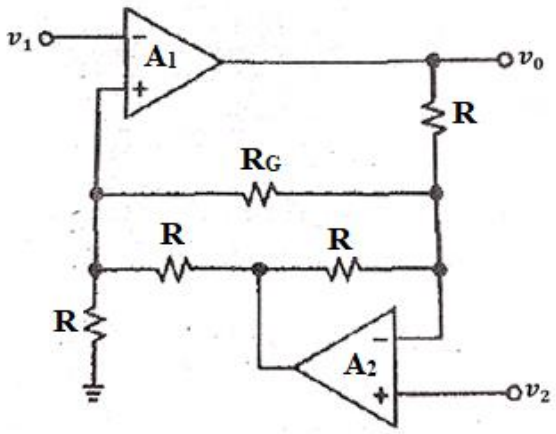

Fig. Q2A

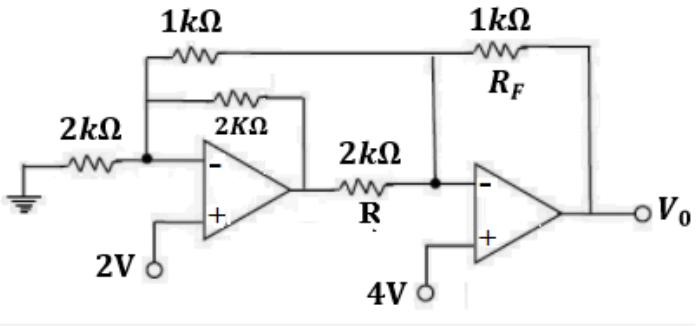

Fig. Q2B

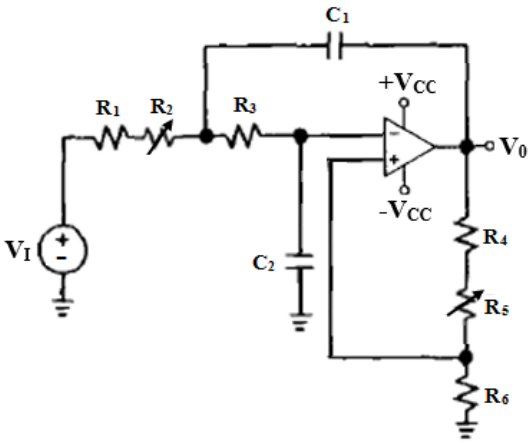

Fig. Q3A

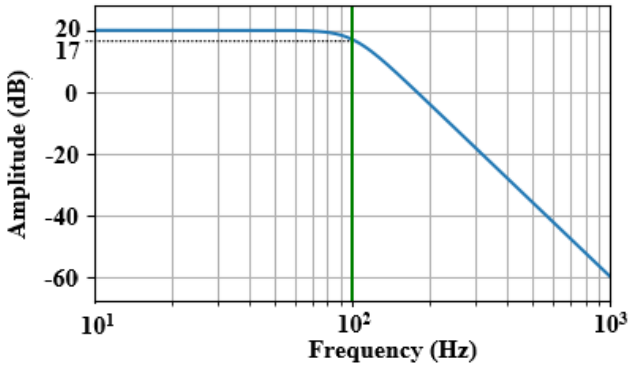

Fig. Q3B(i)

n	Normalised Denominator Polynomials in Factored Form				
1	(1+s)				
2	(1+1.414s+s²)				
3	(1+s)	(1+s+s²)			
4	(1+0.765s+s²)	(1+1.848s+s²)			
5	(1+s)	(1+0.618s+s²)	(1+1.618s+s²)		
6	(1+0.518s+s²)	(1+1.414s+s²)	(1+1.932s+s²)		
7	(1+s)	(1+0.445s+s²)	(1+1.247s+s²)	(1+1.802s+s²)	
8	(1+0.390s+s²)	(1+1.111s+s²)	(1+1.663s+s²)	(1+1.962s+s²)	
9	(1+s)	(1+0.347s+s²)	(1+s+s²)	(1+1.532s+s²)	(1+1.879s+s²)
10	(1+0.313s+s²)	(1+0.908s+s²)	(1+1.414s+s²)	(1+1.782s+s²)	(1+1.975s+s²)

Fig. Q3B(ii)

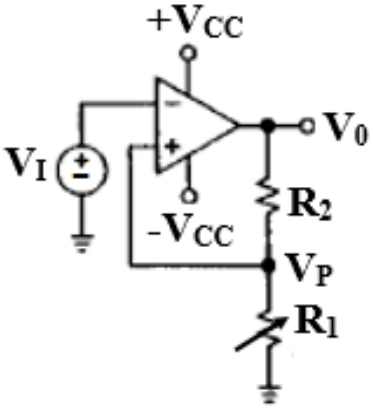

Fig. Q4A

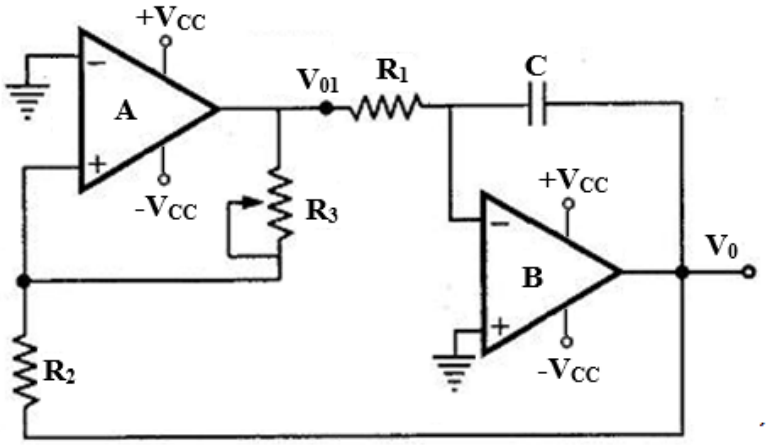

Fig. Q4B

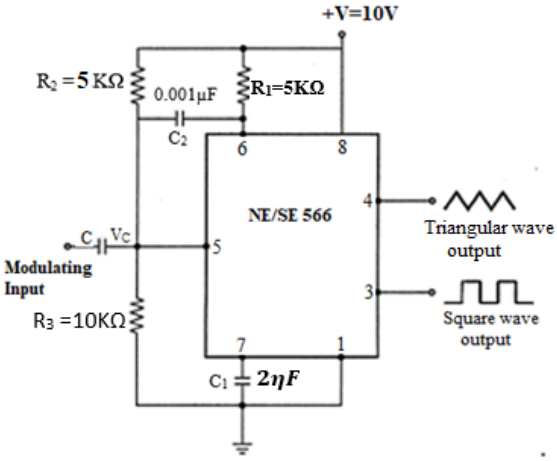

Fig. Q5B