Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

IV SEMESTER B.TECH. (INFORMATION TECHNOLOGY)
GRADE IMPROVEMENT/MAKEUP EXAMINATIONS, AUGUST 2021

SUBJECT: Computer Organization and Microprocessor systems

[ICT 2256]

REVISED CREDIT SYSTEM

(06/08/2021)

Time: 2 Hours MAX. MARKS: 40

Instructions to Candidates:

- Answer **ANY FOUR FULL** questions.
- Missing data may be suitably assumed.

1A.	Mention the addressing modes and write suitable instructions to perform the following a. A 16-bit data has to be read to CX register from an external device with port address 96H b. A 16-bit data from the offset 7860H is to be copied to stack without using PUSH instruction. Assume the initial value of SP to be FFFAH	6
1B.	Explain the following instructions with an example for each a. RCR b. IMUL c. AAD d. MOVSB	4
2A.	Explain the following pins of 8086 microprocessor: READY ii. RESET iii. HOLD iv. NMI v. $\overline{DEN}$ vi. ALE	6
2B.	Assume the priority of I0<I1<I2 and they occur simultaneously. How 8086 and 8259 does handle these hardware interrupts of different priority?	4
3A.	Write an 8086 program to find the square of a 2-digit decimal number available in the data segment and display the decimal result on the screen.	6
3B.	Explain the following assembler directives a. ASSUME b. SEGMENT c. END d. PTR	4
4A.	With necessary waveforms, explain various modes of operation of 8254.	6
4B.	The parameters of a computer memory system are specified as follows: Main memory size = 32K blocks Cache memory size = 1024 blocks Block size = 32 words Determine the size of the tag field of the main memory address for the following mapping techniques: i. Fully associative mapping ii. Direct mapping iii. Set associative mapping with 16 blocks/set.	4

5A.	Write the flow chart of Booth's algorithm. Given M = $15_{(10)}$ and Q = $-17_{(10)}$, perform multiplication using Booth's algorithm indicating all the steps.	6
5B.	With neat diagrams, explain polled and daisy chain techniques for servicing multiple interrupts.	4
6A.	Explain hardwired and microprogrammed control unit design methods with the help of a neat diagram.	6
6B.	Explain cycle – stealing, interleaved and block transfer DMA techniques with necessary diagrams.	4