Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

FIRST SEMESTER M.TECH. (ME/DEC) DEGREE END SEMESTER EXAMINATION
JULY 2021
SUBJECT: DIGITAL VLSI DESIGN (ECE - 5152)

TIME: 2 HOURS **MAX. MARKS: 40**

Instructions to candidates
- Answer any **FOUR Full** questions.
- Missing data may be suitably assumed.

1A. Discuss CMOS inverter with the help of circuit and VTC highlighting the impact of beta ratio on the performance of the circuit.

1B. Estimate the raise time and fall time of a CMOS inverter and establish the condition for obtaining symmetrical operation.

(5+5)

2A. With the help of neat diagrams explain the fabrication of CMOS inverter using SOI process. What are its merits and demerits?

2B. i) Describe Latch-up phenomenon in bulk CMOS.
ii) List the major sources of latch up and the remedies employed to prevent latch up.

(5+5)

3A. With the help of suitable diagrams explain the key timing parameters related to sequential logic and explain the impact of the same on the circuit performance.

3B. With the help of neat diagrams explain clock distribution techniques. Also discuss their salient features.

(5+5)

4A. i) Explain various technology scaling approaches and compare them.
ii) Illustrate the impact of full scaling on Current density and Power delay product.

4B. Discuss any two techniques used to drive large capacitive loads in VLSI and compare them.

(5+5)

5A. Show the complete architecture of 4 MB SRAM memory assuming that the architecture has 16 blocks/banks, and each block is square in shape.

5B. Discuss the working of 3T DRAM cell with the help of circuit and necessary waveforms. Highlight its salient features.

(5+5)

6A. Implement XOR logic using i) Pseudo NMOS and ii) Dynamic CMOS logic. Also compare the circuits taking static CMOS as a reference.

6B. i) What is the need for design rules? Give reasons.
ii) Explain different types of design rules and compare them.

(5+5)