Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

FIRST SEMESTER MTECH. (DEC / ME) DEGREE END SEMESTER EXAMINATION
AUGFUST 2021
SUBJECT: PROCESSOR ARCHITECTURE & APPLICATIONS (ECE - 5154)

TIME: 2 HOURS **MAX. MARKS: 40**

Instructions to candidates
- Answer **ANY FOUR** full questions.
- Missing data may be suitably assumed.

1A. What are the different protocols used for enforcing coherence in centralized share memory architecture? Discuss with examples.

1B. Write programming model/architecture of MSP 430 microcontroller. application.

(5+5)

2A. With a schematic diagram, show pipelined dependencies in a five – instruction sequence given below, using simplified data paths. How these dependencies are resolved via forwarding?

```
sub  $2,  $1,  $3
and  $12,  $2,  $5
or  $13,  $6,  $2
add  $14,  $2,  $2
sw  $15, 100 ( $2)
```

2B. With a diagram, explain MAC unit of a DSP Processor for two 16 bit inputs. If sum of 256 products are to be computed using MAC, with execution time 100 n sec, compute total time to complete the operation. Modify the MAC unit to prevent overflow condition.
A 8 tap FIR filter with maximum sampling time = 1/8T. Show the implementation of the filter with necessary diagram.

(5+5)

3A. Describe architectural overview, on chip memory of TMS320C67x DSP Processor.

3B. Explain DMA based I/O strategy with algorithm / program used for implementation.

(5+5)

4A. Write table showing control values for the forwarding multiplexers from hardware forwarding unit and algorithm / pseudo code for EX and MEM hazards. Sketch forwarding unit with inputs and outputs.

4B. With a diagram, show complete single cycle data path implementation scheme for R – type, load store and branch equal instructions.

(5+5)

5A. With necessary sketches, explain mechanism to map main memory to cache using direct mapping. Discuss its disadvantage. How it can be improved by set associative mapping?

Explain with examples.

5B. What are the taxonomy of parallel processor architectures? Explain. Also discuss processor interconnect strategy for different memory architectures.

(5+5)

6A. Interface 4K byte ROM using address decoder and other logic circuits. Address range is 00006000H to 00006FFFH.

6B. Write JUMP instruction bit format. Show a sketch with the blocks relevant to jump instruction only.

(5+5)