Question Paper

MANIPAL ACADEMY OF HIGHER EDUCATION

MANIPAL SCHOOL OF INFORMATION SCIENCES, MANIPAL
FIRST SEMESTER MASTER OF ENGINEERING - ME (VLSI DESIGN) DEGREE EXAMINATION - FEBRUARY 2021

Verification [EDA 603]

Marks: 100   **Duration: 180 mins.**

MONDAY, FEBRUARY 15, 2021

Answer all the questions.

1)	Discuss the different verification challenges. (TLO-1.1)	(10)
2)	What is Verification? What is being Verified in following Verification Processes. (TLO-2.1) (5+5=10 Marks)	(10)
	a.Formal Verification b.Functional Verification	
3)	Explain the following verification types . (TLO-2.5) (5+5= 10 Marks)	(10)
	a. Black Box Verification b. White Box Verification	
4)	Explain the following verification approaches. (TLO-3.1) (5+5=10 Marks)	(10)
	a.Top-down Verification b.System-interface driven Verification	
5)	Describe the Architecture of Test Bench with neat diagram. (TLO-5.1)	(10)
6)	Write a Verilog code for 4-bit ALU? Write a Self Checking TestBench for above code. (TLO-5.8)	(10)
7)	What is code coverage? Explain different types of code coverage's. (TLO-7.3) (2+8=10 marks)	(10)
8)	Describe interface block in SystemVerilog and mentions its advantages. (TLO-9.1)	(10)
9)	Explain the following with example. (TLO-10.2) (5+5=10 Marks)	(10)
	a. Inheritance b. Polymorphism	
10)	Explain the following with examples . (TLO-10.3) (5+5=10 Marks)	(10)
	a. rand and randc b. rand_mode	

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