Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

FIFTH SEMESTER BTECH. (E & C) DEGREE END SEMESTER EXAMINATION
MARCH 2021
SUBJECT: MICROPROCESSORS (ECE - 3153)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Consider the following code.

```
AREA SUMUP, CODE, READONLY
ENTRY
MOV R1, #2
MOV R2, #9
MOV R3, #45
B SUM
SUBS R1, R1, #1
CMP R1, #0
SUM ADD R1, R2, R3
```

How many clock cycles are required to complete the execution of the above code on non-pipelined processor assuming each instruction will take 3 cycle to execute completely? Show calculations.

How many clock cycles are required to complete the execution of the above code on 3-staged pipelined processor? Draw the pipeline diagram for the same. Let one stage requires one clock cycle and assume all memory references hit in cache.

1B. Describe the functions of GLOBAL and IMPORT directives with proper syntax? Demonstrate the use of these directives by writing an ARM assembly language program to find the product of two 8-bit numbers using repetitive addition. In the main program do all initialization and write subroutine as an external module to find the product.

1C. Explain the two ways of specifying target address in a processor with illustrations and examples. Also mention the advantages and/or disadvantages of each of the methods.

(4+3+3)

2A. A string is stored in a memory with a variable name "STR_NAME" terminated by NULL character. Write an ALP to check whether the given string is palindrome or not. If it is palindrome, store 0x1111, otherwise 0xFFFF as result in memory with a variable name "RESULT".

2B. The operation code of an ARM 7 instruction is 0xE4118004. Identify and explain the function of the above instruction. Also mention the type of addressing mode employed.

2C. What are the different types of stacks supported by ARM 7 processor? Describe the functions of non-empty stack operation with relevant example.

(4+3+3)

3A. Consider the following PRE condition for all the instructions:

R0=0x40000000 R1=0x12345678 R2=0xAABBCCDD
R3=0x1A2A3B4C R4=0x12345678 R5=0x00000000
R6=0x45129860 R7=0x88772344 R8=0xABCDEF34
0x40000000: 0x85 0x76 0x9A 0x23 and C flag =1

Describe the function of following instructions and also specify the post condition:

i. LDRSB R1, [R0], #1
ii. SBC R2, R3, R4, LSR #4
iii. EOR R5, R6, R7, LSR #8
iv. MLA R8, R7, R2, R3

3B. Write a single ARM instruction to perform each of the following tasks.

	Precondition	**Postcondition**
i.	R1=0xABCDDCBA R2=0xFFFFBAFF	R1=0xABCDDCBA R2=0xFFFFFFDD
ii.	R1=0x80000005	R1=0xA0000001
iii.	R0=0x00000002 R1=0x03210321 R2=0x00110011 R4=0x0000000F	R0=0x00000002 R1=0x03430343 R2=0x00110011 R4=0x0000000F

3C. Given below is an assembly language program and the corresponding Disassembly of each instruction. Fill in the missing data in the Disassembly in hexadecimal format, assuming that the first instruction after ENTRY starts at 0xA000F020.

TEMP EQU 82	
AREA Prog3, CODE, READONLY	
ENTRY	
MOV R0, #3	E3A00003: MOV R0, #0x00000003
BL *ARITH1*	EB000000: BL _____
STOP B *STOP*	EAFFFFFE: B _____
LTORG	
ARITH1	
CMP R0, #TEMP	E3500052: CMP R0, _____
BHS ADD1	2A000002: BCS _____
ADR R3, *TABLE*	E28F3000: ADD R3, PC, _____
LDR R2, =0x87654321	E59F2008: LDR R2, [PC, _____]
TABLE	

DCW 0x0003	00000003
ADD1	
ADD R0, R1, R2	E0810002: ADD R0, R1, R2
MOV PC, LR	E1A0F00E: MOV PC, R14
END	

(4+3+3)

4A. List the steps taken up by the processor while returning from an exception in the case when the return address is saved on stack.

4B. What are memory mapped peripherals? Describe the memory map of LPC2132 with the help of a neat diagram.

4C. Observe the below memory addresses of registers in LPC2104 and the values they contain after step-by-step execution of certain instructions. Describe the sequence of actions, the programmer intends to perform in each step, specifying the registers used and the function of the bits.

0xE000C004: 0x03

0xE000C014: 0x20

0xE000C008: 0x04

0xE000C000: 0x0A

0xE000C00C: 0x85

0xE000C000: 0x61

(4+3+3)

5A. Write a C program for OMAP L138 to:

i. Generate a sinusoidal signal of 3 kHz without using lookup table.

ii. Filter the sinusoidal signal generated above using a moving average filter.

5B. Describe the seven operating modes of ARM7TDMI processor. Also show the register file, along with the banked registers for each mode.

5C. Write a C program to create a fading echo effect on the input audio signal using OMAP L138. Assume that only 50% of the output signal is fed back to the input.

(4+3+3)