Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

FIFTH SEMESTER BTECH. (E & C) DEGREE END SEMESTER EXAMINATION
JANUARY/FEBRAURY 2021
SUBJECT: MICROPROCESSOR (ECE - 3153)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Consider the following code:

```
        AREA  ASCENDING, CODE, READONLY
        ENTRY
        MOV R8, #2
LOOP0   LDR R1, [R2], #4
        STR R1, [R3], #4
        SUBS R8, R8, #1
        CMP R8, #0
        BNE LOOP0
```

How many clock cycles are required to complete the execution of the above code on non-pipelined processor assuming each instruction will take 1 cycle to execute completely? Show calculations.

How many clock cycles required to complete the execution of the above code on 3-staged pipelined processor? Draw the pipeline diagram for the same. Let one stage requires one clock cycle and assume all memory references hit in cache.

1B. Explain macros and subroutines with proper syntax. Write a macro-based assembly program to find the GCD of two 32-bit numbers.

1C. Explain interrupt vector and IVT in ARM. Write the IVT of ARM7, showing priorities and vector addresses for all the interrupts.

(4+3+3)

2A. Given that a word is stored in the memory with a variable name “NUM”, write an ALP to check whether the given word is bitwise palindrome or not. If it is palindrome, store the condition 0x1111, otherwise 0xFFFF as result in memory with a variable name “RESULT”.

2B. Assume that the main program and subroutines uses all the registers to store certain values. Let us consider a situation in which a main program calls a subroutine and this subroutine calls another subroutine. Describe with complete coding example to add array of 32-bit numbers stored in a memory terminated by ‘0’. In first subroutine find the number of words and in the second subroutine find the sum and store the result in memory. Demonstrate how your code determine its way back to the calling main program without destroying registers contents?

2C. Explain the pseudo instruction which is used to load address into destination register. What is the addressing mode associated with it. Describe in detail with an example.

(4+3+3)

3A. Describe the functions of following instructions in detail. Also identify the type of addressing mode and result after execution of each instruction for the given pre condition:

i. SMLAL R3, R5, R6, R8

ii. STMIB R1!, {R1-R4}

iii. MOVS R2, R4, LSR R0

iv. RSC R0, R81, R7, LSR #8

Given pre condition:

R0 = 0x40000000 R1 = 0x12345678 R2 = 0xAABBCCDD

R3 = 0x1A2A3B4C R4 = 0x12345678 R7 = 0x88772344

R8 = 0xABCDEF34

3B. Write a single ARM instruction to perform each of the following tasks.

	Precondition	**Postcondition**
i.	R1=0x01234567 R2=0x01234567 CPSR=0x000000D3	R1=0x01234567 R2=0x01234567 CPSR=0x400000D3
ii.	R1=0x01234567 CPSR=0x000000D3	R1=0x000000D3 CPSR=0x000000D3
iii.	R0=0x00000001 R1=0x00112233 R2=0x03210321 R4=0x0000000F	R0=0x00000002 R1=0XF6420651 R2=0x03210321 R4=0xF000000F

3C. A 32-bit Gray code stored in the memory as GRAY_CODE, write an ALP to convert it into its equivalent Binary code and store the result in memory as BINARY_CODE. Don't use table method.

(4+3+3)

4A. Given below is an assembly language program and the corresponding Disassembly of each instruction. Fill in the missing data in the Disassembly in hexadecimal format, assuming that the first instruction after ENTRY starts at 0xA006C01C.

NUM EQU 2	
AREA Prog, CODE, READONLY	
ENTRY	
MOV R0, #3	E3A00003: MOV R0, #0x00000003
MOV R1 ,#58	E3A0103A: MOV R1, ……..
BL *ARITH1*	EB000000: BL ……..
STOP B STOP	EAFFFFFE: B ……..
LTORG	
ARITH1	
CMP R0, #NUM	E3500002: CMP R0, ……..
BHS *ADD1*	2A000003: BCS ……..
ADR R3, TABLE	E28F3004: ADD R3, PC, ……..
LDR PC, [R3, R0, LSL #2]	E793F100: LDR PC, [R3, R0, LSL #2]
LDR R2, =0x87654321	E59F2008: LDR R2, [PC, ……..]
TABLE DCW 0x0001, 0x0002	00020001: ANDEQ R0, R2, R1
ADD1	

ADD R0, R1, R2	E0810002: ADD R0, R1, R2
MOV PC, LR	E1A0F00E: MOV PC, ……..
END	87654321: STRHIB R4, [R5,-R1,LSR #6]!

4B. Given the input voltage of DAC in LPC2132 is 0x3E8, settling time is 2.5 microsecond and the maximum current is 350 microampere. Write the corresponding bit format of the DAC register, with the help of a neat diagram and explain. If the reference voltage of the DAC is 3V, what will be the output analog voltage?

4C. Observe below the memory addresses of registers in LPC2104 and the values they contain after step-by-step execution of certain instructions. Describe the sequence of actions the programmer intends to perform in each step, specifying the registers used and the function of the bits.

0xE000C00C: 0x83
0xE000C000: 195
0xE000C004: 0x0
0xE000C00C: 0x03
0xE000C004: 0x03
0xE000C000: 0xFF

(4+3+3)

5A. With a neat diagram, explain ARM core dataflow model. Describe the different types of barrel shift operations with relevant diagram.

5B. Write a C program to generate the following signals using OMAP L138:
i. Square wave ii. Ramp signal

5C. Write a C program to read a 1-channel audio signal and add a delay of 0.25 seconds to this signal using OMAP L138.

(4+3+3)