Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SEVENTH SEMESTER BTECH. (E & C) DEGREE END SEMESTER EXAMINATION
JANUARY/FEBRUARY 2021
SUBJECT: RTL VERIFICATION USING VERILOG (ECE - 4021)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Find the essential prime implicant for the set of prime implicants F={C_1, C_2, C_3, C_4, C_5} where F (A, B, C, D) = ∑m (1, 2, 3, 4, 5) using ESPRESSO algorithm.

1B. Draw ROBDD for 3 bit even number counter. Show all the steps. Also perform ITE algorithm for OBDD.

1C. Write the Verilog AMS code for the given expression to calculate $P = I^2R$. Use parameter declaration. The values can be suitably assumed.

(4+3+3)

2A. Draw the sequencing graph for the circuit shown in **Fig. 2A**. Apply Clique partitioning algorithm for the sequencing graph and determine the operation binding resources for MUL and ALU. Show all the steps. Assume only two input operations are available in the sequencing graph.

2B. Find out the prime implicants for the following expression using Iterative consensus method.

F= $A'C'D' + AB + CD + ACD$

2C. Draw control and data flow graph for the given sequential statement:
if $(A * B) < (C * D)$ then $F = Q - P$; else $F = P - Q$; where $P = A * B$; $Q = C * D$

(4+3+3)

3A. Draw the sequencing graph for the circuit given in **Fig. 2A**. Assume the execution delays of the multiplier and the ALU are 4 and 2 cycle respectively. Calculate mobility using ALAP algorithm. Also determine the number of resources using Hu algorithm. Assume P(0)=1; P(1)=3; P(2)=4; P(3)=2; P(4)=2. If any other P values exists, it needs to be assumed as 2. Draw the rescheduled graph. Assume only AND, OR, INVERTER operations are available in sequencing graph.

3B. Write the Verilog AMS code for Voltage follower circuit. The values can be suitably assumed.

3C. Draw a OBDD graph for $F = AB + BC + CA$ in the order of $B - C - A$.

(4+3+3)

4A. Draw the sequencing graph for the given block shown in **Fig. 4A**. Calculate mobility using ALAP algorithm. Assume unit execution delay. Apply LIST-L Scheduling algorithm for the sequencing graph. Draw the scheduled graph under resource constraints. Assume only AND, OR, INVERTER operations are available in sequencing graph.

4B. Write the behavioural VHDL code for determining 2's complement of a given 6 bit binary number.

4C. Draw RTL schematic and technology schematic for half adder. Assume Xilinx FPGA is chosen and the functional unit of Xilinx FPGA is Lookup table (LUT).

(4+3+3)

5A. Write the sequential VHDL code for the given circuit shown in **Fig. 5A.**

5B. Draw the reduced state diagram for the given state diagram shown in **Fig. 5B.**

5C. Draw ROBDD for 4:1 multiplexer using 2:1 multiplexer. Assume only AND, OR and NOT gates are available. Also assume real and complement of the input variable is already available. Perform ITE for BDD.

(4+3+3)

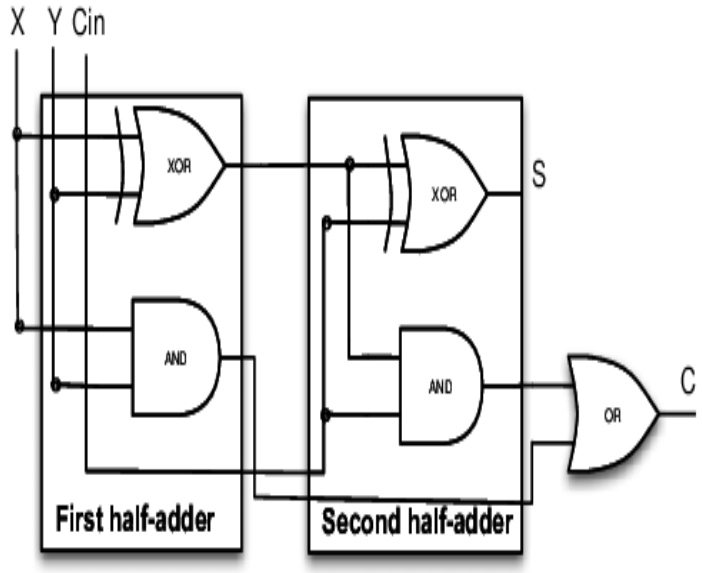

Fig. 2A

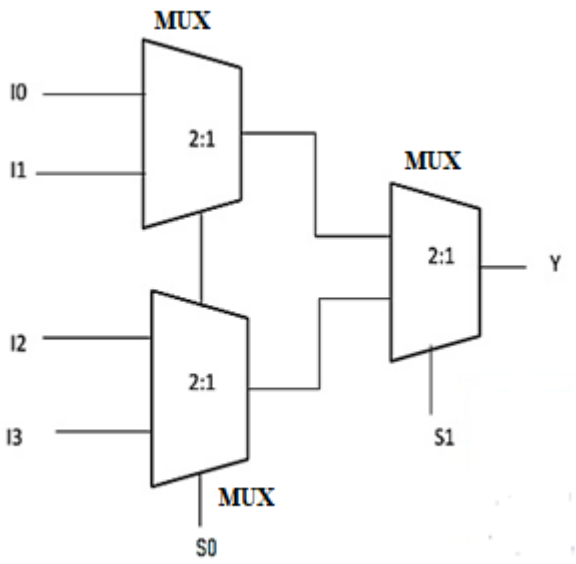

Fig. 4A

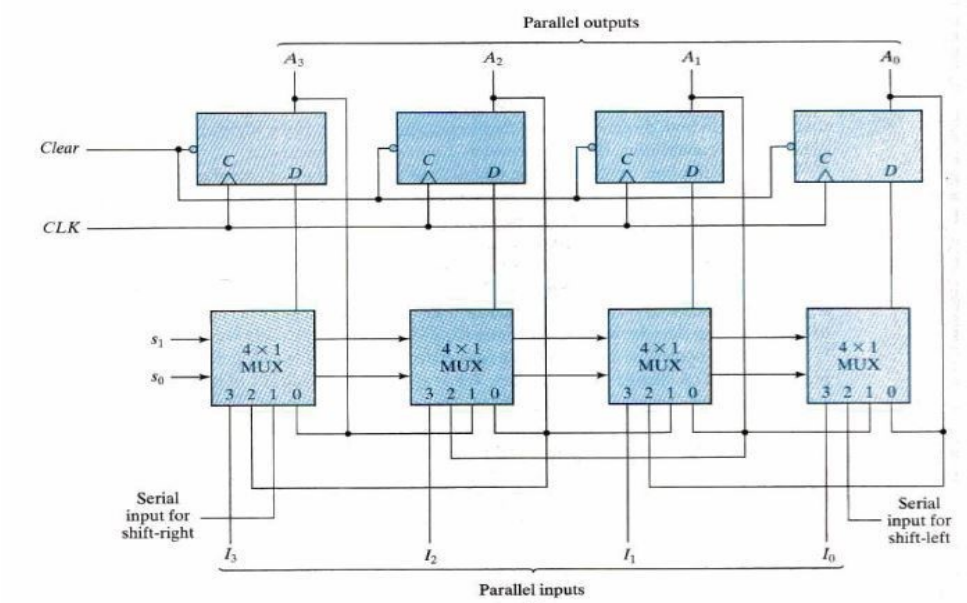

Fig. 5A

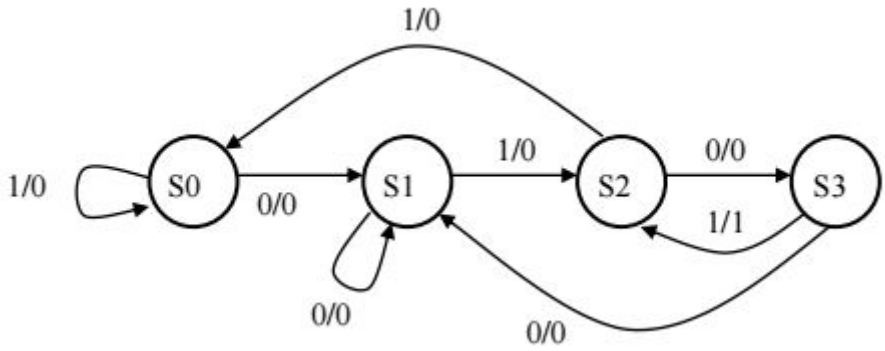

Fig. 5B