Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

VII SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

ONLINE EXAMINATIONS, JANUARY- FEBRUARY 2021

FPGA BASED SYSTEM DESIGN [ELE 4002]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 27 January 2021** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. With circuit diagram explain how pass transistor, transmission gate, multiplexer, and switching matrix based routing is controlled using SRAM programming technology. What are the advantages with transmission gate over pass transistor routing architecture? ***(04)***

1B. Explain with diagrams the design steps involved with partial run time reconfiguration of FPGAs. Also mention benefits of run time reconfiguration. ***(04)***

1C. What are the benefits of using a soft embedded processor in an FPGA over a hard-macro implementation? ***(02)***

2A. Consider the circuit shown in **Fig Q2A**. Determine the circuit which is functional equivalent to **Fig Q2A** (modify the given circuit) and also should be tested easily for s-a-1 and s-a-0 faults. Justify the answer. ***(05)***

2B. A jet aircraft employs a system for monitoring the RPM, pressure and temperature values of its engines using sensors that operate as follows: ***(05)***

R sensor output = 0 only when speed < 4800 rpm

P sensor output = 0 only when pressure < 220 psi (pound per square inch)

T sensor output = 0 only when temperature < 220° F

Design a logic circuit that controls a cockpit warning light for the following combinations of the engine conditions:

Temperature is higher than the threshold and either speed is lower or pressure is higher than the given threshold value.

The signal controlling the cockpit warning light is checked for every 1 minute. Assume there exists a system that generates signal with appropriate frequency.

Also, implement the designed circuit on the given FPGA. The FPGA layout and CLB details are given the **Fig Q2B**. Determine the generated configuration bitstream for all the configurable elements. Do not include configurable bits for generating the 1-minute signal.

Assume six pass transistors per switch block (SB). Name all the pass transistors in switch block. Accordingly write the bit pattern for switch blocks.

3A. Block diagram of the serial adder is shown in **Fig Q3A**. Implement the same using Actel ACT-2 modules. ***(04)***

3B. A digital system is required to control an automatic sliding door with the following conditions. An input 'p' to the digital system indicates whether a sensor detects a person in front of the door. An input 'q' indicates whether the door should be manually held open regardless of whether a person is detected. An input 'r' indicates whether the door should be forced to stay closed. r=1 means the door should stay closed. Assume a Verilog module is available describing the behavior of the digital system. Write the Verilog self-checking test bench code to check the functionality of the Verilog module. Check for all the combinations of the inputs. ***(03)***

3C. A sequential circuit has the following Boolean equations for next state decoder and output Z: ***(03)***

$$D_1 = Q_2\bar{X} + Q_1\bar{Q}_2X\ (MSB)$$
$$D_2 = X$$
$$Z = Q_1Q_2$$

Determine the shortest input sequence that will distinguish the state transitions. Also verify all state transitions from any one of the states.

4A. Design a system for an automobile that illuminates a warning light with initial illumination. Warning light is turned on whenever a person is actually sitting in the driver's seat, the driver's seatbelt is not fastened, and the key is in the ignition. To provide the initial illumination warning light should be turned ON when you first turn the key so that one can check whether the warning light is working. For this there exists a system that generates signal that is 1 for first 5 seconds after key is inserted into the ignition, and 0 afterward. Implement the circuit using combinational circuit and draw the stick diagram for the same. ***(04)***

4B. Implement digital circuit to add two 4-bit number in Spartan 2E FPGA using ***(06)***

i. LUTs only
ii. LUTs and dedicated mux
iii. LUTs and carry control logic

In each case calculate the number of LUTs needed, levels of logic, and the number of CLBs required for the implementation?

5A. Provide the data path for the following problem statements. Clearly mention the digital components and connections between components (including width of wires). ***(05)***

i) A home entertainment center has four different audio sources that can be played over the same set of speakers. Each audio source, named A, B, C, and D, is connected using 8 wires on which the digitized audio signal is transmitted. The user selects the audio source using a rotary switch with four outputs S_0, S_1, S_2, and S_3, of which exactly one will be '1' at any given time. If S_0 = '1', the audio source A should be played, if S_1 = '1', the audio source B should be played, and so on.

ii) Computing the minimum of two 8-bit numbers.

5B. The impulse response of a linear phase FIR filter is h(n)=[**1** 2]. Develop FPGA based architecture for two-bit parallel distributed arithmetic FIR filter. Explain the developed architecture. Determine response of developed filter for the input x(n)=[**4** 5]. Clearly with explanation mention the partial output for each bit shift of the shift register. ***(05)***

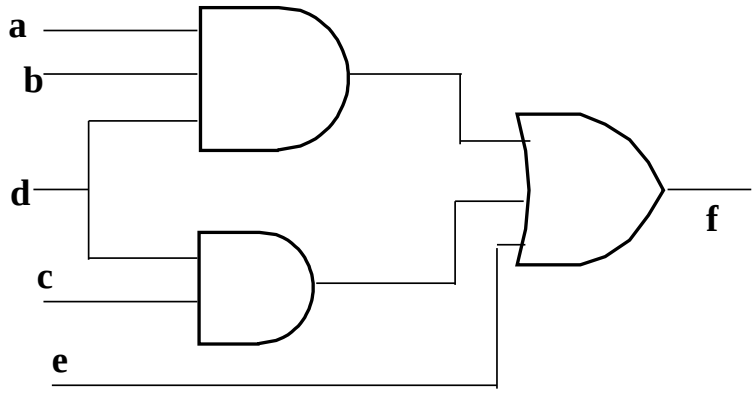

Fig Q2A

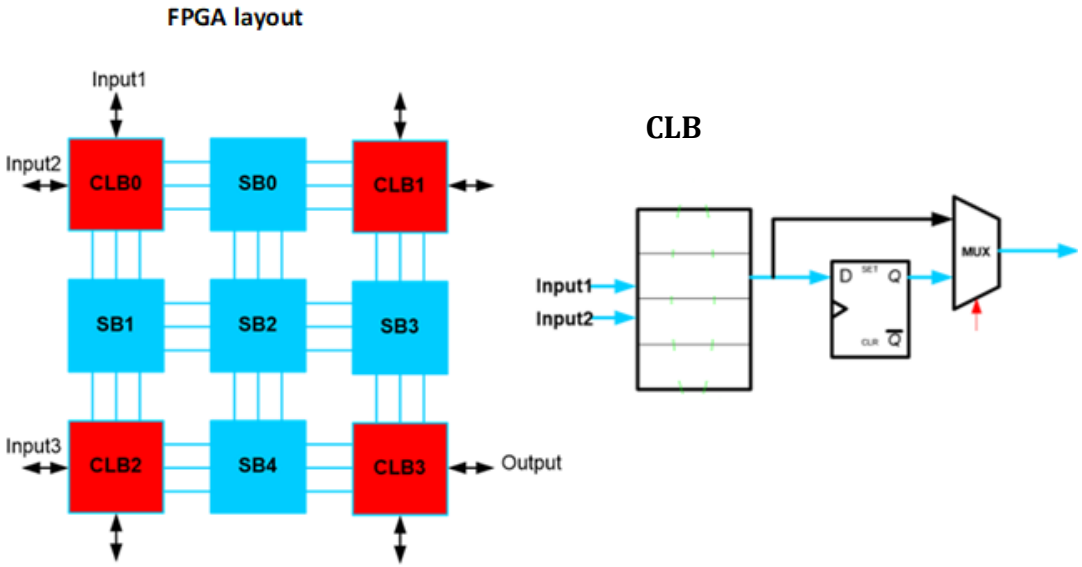

Fig Q2B

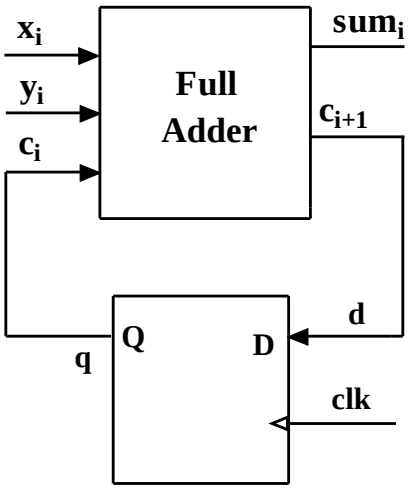

Fig. Q3A