Reg. No.											

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

III SEMESTER B.TECH. (COMPUTER AND COMMUNICATION ENGINEERING)
END SEMESTER EXAMINATIONS, JANUARY 2022
SUBJECT: Digital Systems and Computer Organization [ICT 2171]
REVISED CREDIT SYSTEM
(22 /01 /2022)
MAX. MARKS: 20

Write Up Time: 9:20 AM to 10:35 AM **Upload Time: 10:35 AM to 10:45 AM**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data, if any, may be suitably assumed.

1A. Design a code converter to convert a decimal digit represented in 8 4 -2 -1 to a decimal digit represented in Gray code using 74138 ICs and minimum external gates. 5M

1B. Divide $14_{(10)}$ by $5_{(10)}$ using restoring division algorithm indicating all the steps. 3M

1C. Explain block transfer DMA technique with a neat diagram. 2M

2A. Design a 4-bit synchronous up counter, using D flipflops, to count the decimal digits in the following sequence. 5M
$0 \rightarrow 9 \rightarrow 2 \rightarrow 8 \rightarrow 3 \rightarrow 7 \rightarrow 4 \rightarrow 6 \rightarrow 5 \rightarrow 0$

2B. Construct a two-digit hexadecimal counter to count from 77H to 38H using 74193 ICs. 3M

2C. Design a asynchronous sequential circuit using JK flipflops and external gates to generate the sequence 10110. 2M

****