

ECE 2151 ANALOG ELECTRONIC CIRCUITS (E&C)

Symbols and Notations:

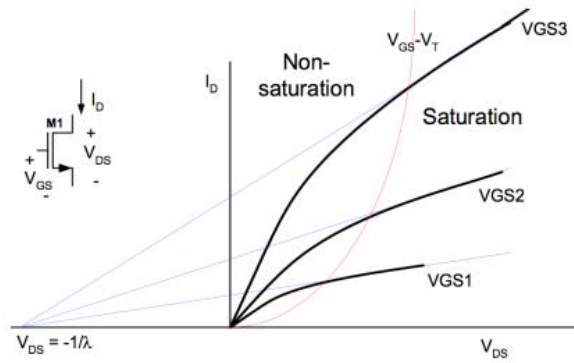
Symbol	Name	Unit
V_T	threshold Voltage	V
V_{GS}	gate to Source Voltage	V
I_{DS}	drain Current	mA
V_{DS}	drain to Source Voltage	V
$\mu_n C_{ox} \frac{W}{L}$		A/V ²
μ_n	mobility of charge carriers	cm ² /(V-s)
C_{ox}	gate capacitance per unit area	F/cm ²
$\frac{W}{L}$	aspect ratio	-
λ	channel-length modulation coefficient	V ⁻¹
gm	trans conductance	S
r_0	mos output impedance	Ω
$C_{Mi} = (1 - A_v)C_f$	milller Capacitance (input)	F
A_v	voltage Gain (Mosfet)	-
C_{Mo}	milller Capacitance (output)	F
A_F	voltage gain with feedback (opamp)	-
S	slew rate	V/ μ S
A_{DM}	Differential mode gain	
A_{CM}	Common mode gain	
K	Feedback factor	
R_{in}	Input resistance without feedback	Ω
R_{out}	Output resistance without feedback	Ω
A_V	Voltage gain without feedback	
A_I	Current gain without feedback	
R_0	Transresistance without feedback	Ω
G_m	Transconductance without feedback	S
H(S)	Transfer function	

MOSFET EQUATIONS:

N channel MOSFET:

Cut off	$V_{GS} \leq V_T$	$I_{DS} = 0$
Linear	$V_{GS} > V_T, V_{DS} \leq V_{GS} - V_T$	$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] (1 + \lambda V_{DS})$
Saturation	$V_{GS} > V_T, V_{DS} > V_{GS} - V_T$	$I_{DS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$

MOSFET Characteristics:



MOS Transconductance:

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$$

$$g_m = \frac{2I_D}{V_{GS} - V_T}$$

MOS Drain to Source Resistance:

$$r_0 \approx \frac{1}{\lambda I_D}$$

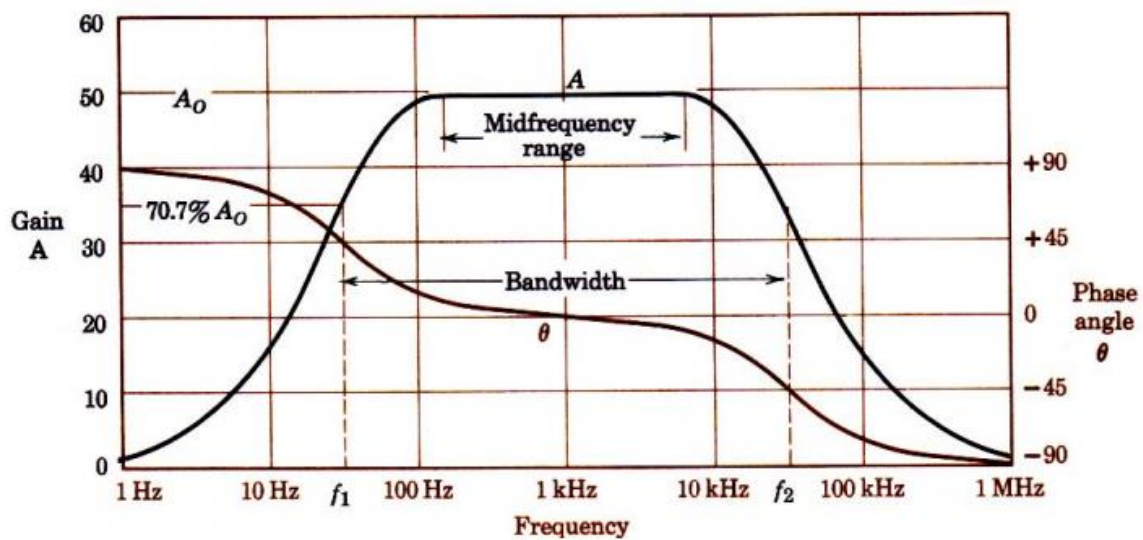
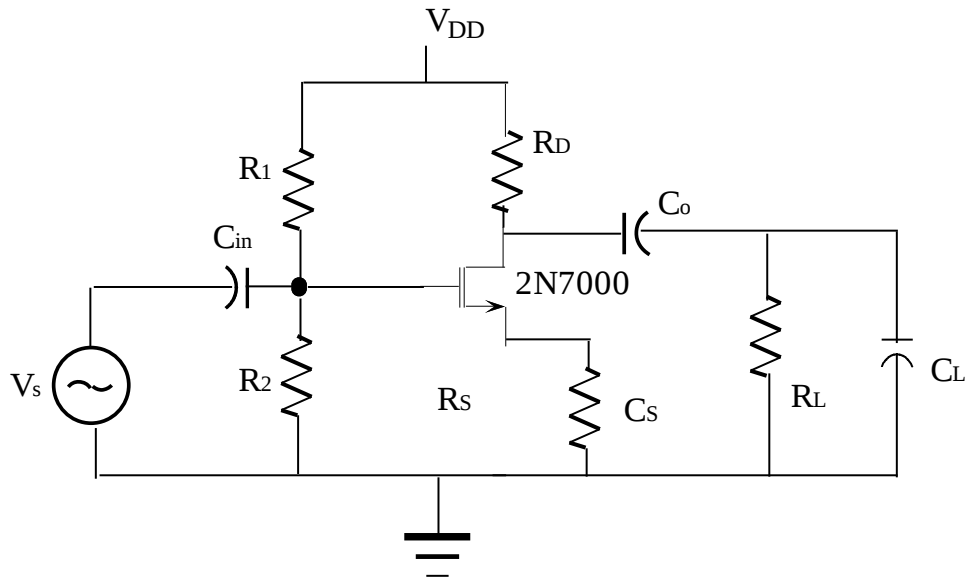
MOS Amplifiers:

Common-source stage	Small-signal model
The circuit diagram shows an n-channel MOSFET M_1 with its gate connected to the input voltage V_{in} and its source connected to ground. The drain is connected to a load resistor R_D and a supply voltage V_{DD}. The output voltage V_{out} is taken from the drain. The drain current is labeled I_D.	The small-signal model consists of an input voltage v_{in} applied to the gate. The gate-source voltage is v_1. A dependent current source $g_m v_1$ is connected between the drain and the source. The drain is connected to a load resistor R_D and the output voltage v_{out} is taken from the drain. The source is connected to ground.

Differential Amplifiers:

Common mode to differential mode conversion (A_{CM-DM}) (effect of asymmetries, for load resistor mismatch)	$\left \frac{\Delta V_{out}}{\Delta V_{CM}} \right = \frac{\Delta R_D}{\frac{1}{g_m} + 2R_{SS}}$
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RC Coupled Amplifier frequency Response:



Determination Of Coupling And Bypass Capacitors:

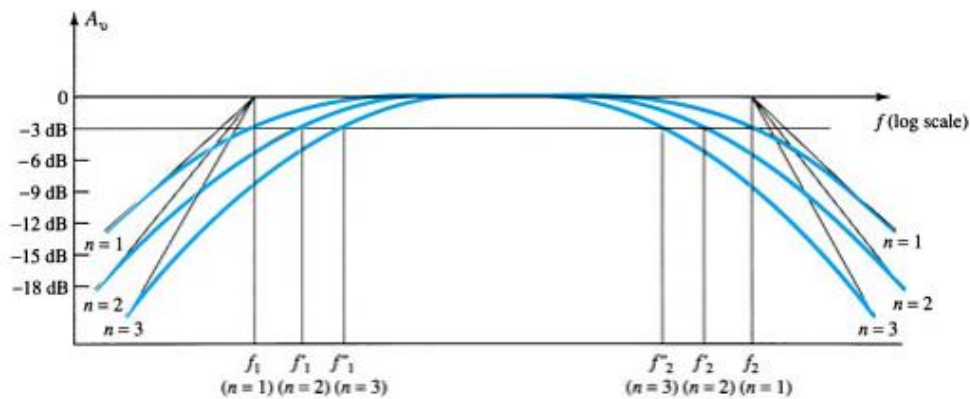
$$X_{Cin} \propto \frac{1}{2\pi f_L C_{in}} \text{ and } X_{Cin} \propto R_i = R_1 \propto R_2$$

$$|X_{Co}| = \frac{1}{2\pi f_L C_o} \text{ and } |X_{Co}| = (R_D \parallel r_o) + R_L$$

$$|X_{CL}| = \frac{1}{2\pi f_H C_L} \text{ and } \propto X_{CL} \propto (R_D \propto R_L \propto r_o)$$

$$|X_{Cs}| = \frac{1}{2\pi f_L C_s} \text{ and } |X_{Cs}| = \left(R_s \parallel \frac{1}{g_m} \right)$$

Multistage Amplifier Frequency Response:



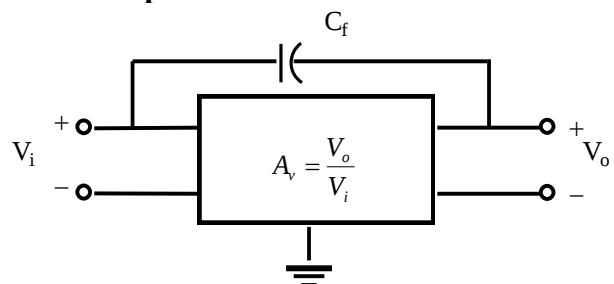
The lower cut off frequency of multistage MOSFET Amplifier is

$$f_1' = \frac{f_1}{\sqrt{2^n - 1}} \quad \text{where } f_1 \text{ is lower cut off frequency of a single stage MOSFET Amplifier}$$

The higher cut off frequency of multistage MOSFET Amplifier is

$$f_2' = f_2 \sqrt{2^n - 1} \quad \text{where } f_2 \text{ is upper cut off frequency of a single stage MOSFET Amplifier}$$

Miller Capacitance:



$$C_{Mi} = (1 - A_v)C_f$$

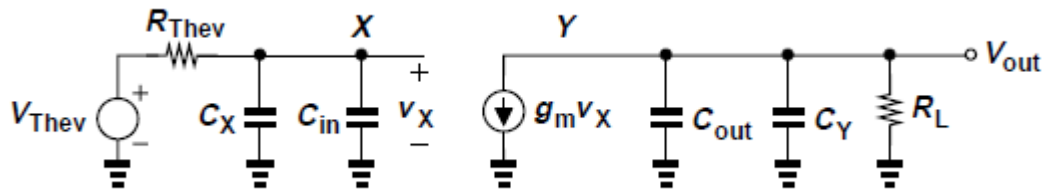
$$C_{Mo} = \left(1 - \frac{1}{A_v}\right)C_f$$

Miller's theorem:

Inverting circuit with floating capacitor	Circuit as obtained from Miller's theorem.

High-Frequency Response

Unified model



Pole frequencies are:

$$|\omega_{pin}|$$

$$|\omega_{pout}|$$

C_{XY} tied between X and Y.

OPAMP CIRCUITS:

Inverting Configuration: $A_F = \frac{-R_F}{R_1}$

Non-Inverting Configuration: $\text{Gain } A_F = 1 + \frac{R_F}{R_1}$

Slew Rate

$$S \frac{\Delta V_O}{\Delta T} \text{ v}/\mu\text{sec}$$

At any frequency f_s , and at a definite gain the maximum value of undistorted output voltage

$$V_{\max} = \frac{S}{2\pi f_s} \text{ v where } S \text{ is the slew rate of the Opamp.}$$

Diode Current $I = I_0 \left(e^{\frac{V}{\eta V_T}} - 1 \right)$	I: diode current I_0 : diode reverse saturation current at room temperature V: external voltage applied to the diode η : = a constant, 1 for Ge, and 2 for Si V_T : Thermal voltage $V_T = kT/q = T/11600$, volt-equivalent of temperature K: Boltzmann's constant (1.38066×10^{-23} J/K) q: charge of an electron (1.60219×10^{-19} C) T: temperature of the diode junction in $^{\circ}\text{K}$ ($273^{\circ} + ^{\circ}\text{C}$)
BJT Fixed Bias $S = 1 + \beta$	S: Stability factor β : Common-emitter current gain
BJT self-bias $S = \left(1 + \beta \right) \frac{1 + \frac{R_B}{R_E}}{1 + \beta + \frac{R_B}{R_E}}$	S: Stability factor β : Common-emitter current gain R_B : Base Resistor R_E : Emitter Resistor
BJT	$I_{B\max}$: Maximum Base current

$I_{Bmax} = \frac{I_{CSat}}{\beta_{dc}}$	I_{CSat} : Collector saturation current β_{dc} : Common-emitter current gain
$P_D = (T_J - T_A) / \Theta_{J-A}$	P_D : Power dissipated in the transistor T_J : Junction temperature in °C T_A : Ambient temperature in °C Θ_{J-A} : Thermal resistance from junction to ambience
$P_D = (T_J - T_C) / \Theta_{J-C}$	P_D : Power dissipated in the transistor T_J : Junction temperature in °C T_C : Case temperature in °C Θ_{J-C} : Thermal resistance from junction to case
$\Theta_{J-A} = \Theta_{J-C} + \Theta_{C-A}$	Θ_{J-A} : Thermal resistance from junction to ambience Θ_{J-C} : Thermal resistance from junction to case Θ_{C-A} : Thermal resistance from case to ambience
Small Signal Model of BJT:	
$r_{ac} = \beta r_e$	r_{ac} : Resistance looking in to the base of transistor β : Common-emitter current gain $r_e = \frac{26mV}{I_E}$; I_E = Emitter current
C.E amplifier in fixed bias circuit	
$Z_i = R_B \vee \beta r_e$	Z_i : Input impedance R_B : Base resistor β : Common-emitter current gain $r_e = \frac{26mV}{I_E}$; I_E = Emitter current
$Z_O = r_O \parallel R_C$	Z_O : Output impedance r_O : Output resistance R_C : Collector resistor
$A_V = \frac{-R_C \vee r_O}{r_e}$	A_V : Voltage gain R_C : Collector resistor r_O : Output resistance $r_e = \frac{26mV}{I_E}$; I_E = Emitter current
CE amplifier in Voltage divider Biasing	
$Z_i = R^1 \vee \beta r_e$	Z_i : Input impedance $R^1 = R_1 \vee R_2$ β : Common-emitter current gain $r_e = \frac{26mV}{I_E}$; I_E = Emitter current
$Z_o = R_C \vee r_o$	Z_o : Output impedance R_C : Collector resistor r_o : Output resistance
$A_v = \frac{-(R_C \vee r_o)}{r_e}$	A_v : Voltage gain R_C : Collector resistor r_o : Output resistance $r_e = \frac{26mV}{I_E}$; I_E = Emitter current
CC configuration	
$Z_i = R_B \vee Z_b$	Z_i : Input impedance R_B : Base resistor
$Z_b = \beta r_e + (1 + \beta)R_E$	Z_b : Impedance looking in to the base terminal β : Common-emitter current gain $r_e = \frac{26mV}{I_E}$

	I_E : Emitter current, R_E : Emitter resistor
$Z_O = r_e \vee R_E$	Z_O : Output impedance $r_e = \frac{26\text{mV}}{I_E}$; I_E : Emitter current R_E : Emitter resistor
$A_v = \frac{R_E}{R_E + r_e}$	A_v : Voltage gain $r_e = \frac{26\text{mV}}{I_E}$; I_E : Emitter current R_E : Emitter resistor
Field Effect Transistor (JFET)	
$\mu = g_m r_d$	μ : Amplification factor g_m : Trans-conductance r_d : Dynamic drain resistance
$I_{DS} = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$	I_{DS} : Drain to source current I_{DSS} : Drain saturation current at pinch-off V_{GS} : Gate to source voltage V_P : Pinch-off voltage (= $ V_{GS(\text{off})} $)
$V_{GS} = V_P \left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$	V_{GS} : Gate to source voltage V_P : Pinch-off voltage (= $ V_{GS(\text{off})} $) I_D : Drain current I_{DSS} : Drain saturation current at pinch-off
$V_{DSmin} = V_{GS} - V_P$	V_{DSmin} : Minimum drain to source voltage V_{GS} : Gate to source voltage V_P : Pinch-off voltage (= $ V_{GS(\text{off})} $)
Enhancement Type MOSFET	
$V_{DS(\text{Sat})} = V_{GS} - V_T$	$V_{DS(\text{Sat})}$: Drain to source saturation V_{GS} : Gate to source voltage V_T : Threshold voltage
$I_D = k$	I_D : Drain Current k : Constant V_{GS} : Gate to source voltage V_T : Threshold voltage
$k = \frac{I_{D(\text{ON})}}{(V_{GS(\text{ON})} - V_T)^2}$	k : Constant $I_{D(\text{ON})}$: Drain current corresponding to $V_{GS(\text{ON})}$ $V_{GS(\text{ON})}$: Gate to source voltage at which channel is ON. V_T : Threshold voltage
Depletion MOSFET	
$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$	I_{DS} : Drain to source current I_{DSS} : Drain saturation current at pinch-off V_{GS} : Gate to source voltage V_P : Pinch-off voltage
FET Amplifiers:	
$g_{mo} = \frac{2I_{DSS}}{V_P \vee}$	g_{mo} : g_m at $V_{GS}=0$ I_{DSS} : Drain saturation current at pinch-off V_P : Pinch-off voltage
$g_m = g_{mo} \left[1 - \frac{V_{GS}}{V_P}\right]$	g_m : Trans-conductance g_{mo} : g_m at $V_{GS}=0$

	V_{GS} : Gate to source voltage V_P : Pinch-off voltage
JFET Fixed Bias circuit:	
$A_v = -g_m(r_d \vee R_D)$	A_v : Voltage Gain g_m : Trans-conductance r_d : Dynamic drain resistance R_D : Drain Resistor
$Z_o = R_D \vee r_d$	Z_o : Output impedance R_D : Drain resistor r_d : Dynamic drain resistance
Self-Bias Configuration:	
$A_v = -g_m(r_d \vee R_D)$	A_v : Voltage Gain g_m : Trans-conductance r_d : Dynamic drain resistance R_D : Drain Resistor
$Z_o = R_D \vee r_d$	Z_o : Output impedance R_D : Drain resistor r_d : Dynamic drain resistance
JFET Self-Bias Configuration (Un-bypassed R_S):	
$Z_o = \frac{1 + g_m R_S + \frac{R_S}{r_d}}{1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}} R_D$	Z_o : Output impedance R_D : Drain resistor r_d : Dynamic drain resistance g_m : Trans-conductance R_S : Source resistor
$A_v = \frac{-g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$	A_v : Voltage Gain g_m : Trans-conductance r_d : Dynamic drain resistance R_D : Drain Resistor R_S : Source resistor
JFET Voltage Divider Configuration:	
$Z_i = R_1 \vee R_2$	Z_i : Input impedance R_1 & R_2 : Resistors in the input circuit
$Z_o = r_d \vee R_D$	Z_o : Output impedance R_D : Drain resistor r_d : Dynamic drain resistance
$A_v = -g_m(r_d \vee R_D)$	A_v : Voltage Gain g_m : Trans-conductance r_d : Dynamic drain resistance R_D : Drain Resistor
JFET Common Gate Circuit:	
$Z_i = R_S \vee \frac{1}{g_m}$	Z_i : Input impedance g_m : Trans-conductance
$Z_o = r_d R_D$	Z_o : Output impedance R_D : Drain resistor r_d : Dynamic drain resistance
$A = \frac{\frac{R_D}{r_d} + g_m R_D}{1 + \frac{R_D}{r_d}}$	A_v : Voltage Gain g_m : Trans-conductance r_d : Dynamic drain resistance R_D : Drain Resistor

Enhancement MOSFET: Drain Feedback configuration	
$Z_i = \frac{R_F}{1 + g_m(r_d \vee R_D)}$	Z_i : Input impedance g_m : Trans-conductance r_d : Dynamic drain resistance R_D : Drain Resistor R_F : Feedback resistor
$Z_o = r_d \vee R_D$	Z_o : Output impedance R_D : Drain resistor r_d : Dynamic drain resistance
$A_v = -g_m(r_d \vee R_D \vee R_F)$	A_v : Voltage Gain g_m : Trans-conductance r_d : Dynamic drain resistance R_D : Drain Resistor R_F : Feedback resistor
Enhancement MOSFET: Voltage-divider configuration	
$Z_i = R_1 \vee R_2$	Z_i : Input impedance R_1 & R_2 : Resistors in the input circuit
$Z_o = r_d \vee R_D$	Z_o : Output impedance R_D : Drain resistor r_d : Dynamic drain resistance
$A_v = -g_m(r_d \vee R_D)$	A_v : Voltage Gain g_m : Trans-conductance r_d : Dynamic drain resistance R_D : Drain Resistor
Frequency Response of amplifiers:	
$\text{dB} = 10\log_{10}\left(\frac{P_2}{P_1}\right)$	dB: gain in decibel P_1 : Input power P_2 : Output power
$f_L = \frac{1}{2\pi(R_S + R_i)C_S}$	f_L : Lower cut-off frequency R_S : Resistance of the signal source R_i : Input resistance C_S : Coupling capacitor in the input circuit

Characteristics	Feedback Topology			
	Voltage - Series	Current - Series	Current - Shunt	Voltage - Shunt
F.B signal X_f	Voltage	Voltage	Current	Current
Sampled Signal X_o	Voltage	Current	Current	Voltage
Signal Source	Thevenin	Thevenin	Norton	Norton
$\beta = X_f / X_o$	V_f / V_o	V_f / I_o	I_f / I_o	I_f / V_o
$A = X_o / X_e$	$A_v = V_o / V_e$	$G_M = I_o / V_e$	$A_I = I_o / I_i$	$R_M = V_o / I_i$
$D = 1 + \beta A$	$1 + \beta A_v$	$1 + \beta G_M$	$1 + \beta A_I$	$1 + \beta R_M$
A_f	A_v / D	G_M / D	A_I / D	R_M / D

R_{if}	R_i / D	R_i / D	R_i / D	R_i / D
R_{of}	$R_o / (1 + \beta A_v)$	$R_o (1 + \beta G_m)$	$R_o (1 + \beta A_i)$	$R_o / (1 + \beta R_m)$
$R'_{of} = R_{of} \parallel R_L$	R'_o / D	$R'_o ((1 + \beta G_m)/D)$	$R'_o ((1 + \beta A_i)/D)$	R'_o / D
$R'_o = R_o \parallel R_L$	$A_v = \lim_{R_L \rightarrow \infty} A_v$	$G_m = \lim_{R_L \rightarrow 0} G_m$	$A_i = \lim_{R_L \rightarrow 0} A_i$	$R_m = \lim_{R_L \rightarrow \infty} R_m$

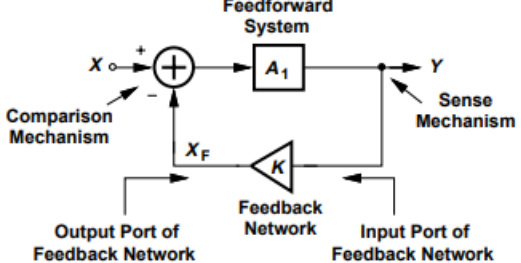
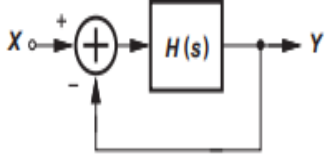
Oscillators:

BJT RC Phase shift oscillator	
$f_o = \frac{1}{2\pi RC\sqrt{6}}$	f_o : frequency of oscillation R: Resistance in the feedback network C: Capacitance in the feedback network
Colpitts Oscillator	
$f_o = \frac{1}{2\pi\sqrt{LC_{eq}}}$	f_o : frequency of oscillation C_{eq} : Equivalent capacitance L: Inductance in the feedback loop
Hartley Oscillator	
$f_o = \frac{1}{2\pi\sqrt{L_{eq}C}}$	f_o : frequency of oscillation L_{eq} : Equivalent inductance C: Capacitance in the feedback loop
Crystal Oscillator	
$f_p = \frac{1}{2\pi\sqrt{LC}}$ $f_p = \frac{1}{2\pi\sqrt{LC_{eq}}}$	f_s : Series resonant frequency L: Inductance C: capacitance f_p : Parallel Resonant Frequency C_{eq} : Equivalent capacitance
Relaxation Oscillator	
$T = 2.303R_E C_E \log_{10} \frac{1}{(1 - \eta)}$	T: Time period R_E : Emitter resistor C_E : Emitter capacitor η : Intrinsic stand-off ratio of UJT

Power Amplifiers:

Parameter	Power Amplifier		
	Class -A	Class-B (Push-pull)	Class-C
Power Output	$P_o = \frac{V_{CEQ} I_{CQ}}{2}$	$P_{o(max)} = \frac{1}{4} V_{CC} i_{C(Sat)}$	$P_{o(max)} = \frac{V_{CC}^2}{2r_c}$
Efficiency (%)	$\eta = \frac{P_{a.c}}{P_{d.c}} \times 100$	$\eta = \frac{P}{P_{d.c}} \times 100$	$\eta = \frac{P_o}{P_i} \times 100$

Power Dissipation	$P_{D(max)} = 2P_{O(max)}$	$P_{D(max)} = \frac{1}{5} P_{O(max)}$	$P_D = \frac{V_{CE(Sat)} \times P_{O(max)}}{V_{CC}}$
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Negative feedback Close loop Gain	 $A_{1,closed} = \frac{A_1}{1 + KA_1}$
Modified Input Impedances of Negative feedback topologies	Voltage - Voltage feedback amplifier: $R_{in,closed} = R_{in}(1 + KA_V)$ Voltage – Current feedback amplifier: $R_{in,closed} = \frac{R_{in}}{(1 + KR_0)}$ Current – Current feedback amplifier: $R_{in,closed} = \frac{R_{in}}{(1 + KA_I)}$ Current – Voltage feedback amplifier: $R_{in,closed} = R_{in}(1 + KG_m)$
Modified Output Impedances of Negative feedback topologies	Voltage - Voltage feedback amplifier: $R_{out,closed} = \frac{R_{out}}{(1 + KA_V)}$ Voltage – Current feedback amplifier: $R_{out,closed} = \frac{R_{out}}{(1 + KR_0)}$ Current – Current feedback amplifier: $R_{out,closed} = R_{out}(1 + KA_I)$ Current – Voltage feedback amplifier: $R_{out,closed} = R_{out}(1 + KG_m)$
Barkhausen Criteria for Oscillation	 $\frac{Y}{X} = \frac{H(S)}{1 + H(S)}$ $ H(S) = 1$ $\angle H(S) = 180^\circ$