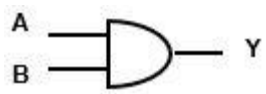
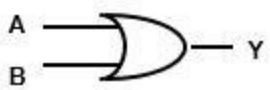
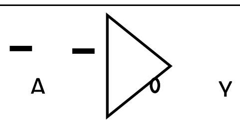
ECE 2153 DIGITAL SYSTEM DESIGN (E&C)

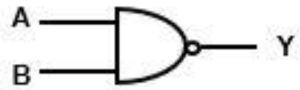
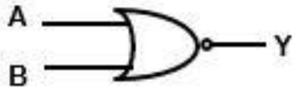
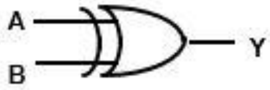
THEOREMS AND POSTULATES OF BOOLEAN ALGEBRA:

Theorem/Postulate	Property	Dual Property
Identity	A+ 0=A	A.1=A
Complement	A+ $\acute{A}$ = 1	$A.\acute{A}$ = 0
Null	A+1 = 1	A.0 = 0
Idempotence	A+A= A	A.A= A
Involution	$\acute{\acute{A}}$ = A	
Commutative	A+B= B+A	A.B=B.A
Associative	(A+B)+C =A+(B+C)	(A.B).C = A.(B.C)
Distributive	A(B+C) = AB+ AC	A+BC=(A+B)(A+C)
Absorption	A+AB=A	A(A+B)=A
Simplification	$A + \acute{A}B = A + B$	$A(\acute{A} + B) = AB$
De Morgan	$(A \acute{+} B) = \acute{A}.\acute{B}$	$(A\acute{.}B) = \acute{A} + \acute{B}$
Shannon's Expansion theorem	$f, \dots, a_i, \dots, a_n) =$ $a_i..f(a_1, a_2, \dots..1, \dots, a_n) +$ $\acute{a_i}.f(a_1, a_2, \dots..,0, \dots., a_n)$	$f, \dots, a_i \dots, a_n) =$ $+f(a_1, a_2, \dots..,0, \dots, a_n).$ $[\acute{a_i} + f(a_1, a_2, \dots,1, \dots., a_n)]$
	F=A.F(A='1')+A'F(A='0') : A='1' (Positive cofactor) A='0' (Negative cofactor)	

Noise Margin High	$V_{NH} = V_{OH(Min)}$- $V_{IH(Min)}$	***V*IL :** The ranges of input voltages (V_{IL}) that can represent an acceptable LOW (logic 0) ***V*IH :** The ranges of input voltages (V_{IH}) that can represent an acceptable HIGH (logic 1) ***V*OL:** The ranges of output voltages (V_{OL}) that can represent an acceptable LOW (logic 0) ***V*OH:** The ranges of output voltages (V_{OH}) that can represent an acceptable HIGH (logic 1)
Noise Margin Low	$V_{NL} = V_{IL(Max)}$- $V_{OL(Max)}$	

LOGIC GATES:

Gates	Symbol	Logical expression
AND		**Y= A.B**
OR		**Y= A+B**
NOT		**Y=** $\acute{A}$

NAND		**Y=** $A\acute{.}B$
NOR		**Y=** $A \acute{+} B$
XOR		$Y = A.\acute{B} + \acute{A}.B = A\oplus B$
XNOR		$Y = \acute{A}.\acute{B} + A.B = A \acute{\oplus} B$

KARNAUGH MAP:

Two – variable K-Map:

1) Sum of product form

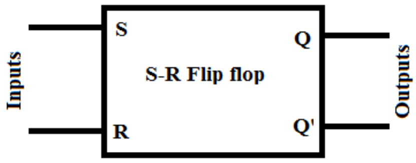
A \ B	$\overline{B}$ 0	B 1
$\overline{A}$ 0	$\overline{A}.\overline{B}$	$\overline{A}.B$
A 1	$A.\overline{B}$	$A.B$

2) Product of sum form

A \ B	B 0	$\overline{B}$ 1
A 0	$A+B$	$A+\overline{B}$
$\overline{A}$ 1	$\overline{A}+B$	$\overline{A}+\overline{B}$

FLIP FLOPS, TRUTH TABLE, EXCITATION TABLE:

<table>
<tr><th>Flip flop</th><th>Truth table</th><th>Excitation table</th></tr>
<tr><td>SR flip flop



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<table>
<tr><th>S</th><th>R</th><th>Q+</th></tr>
<tr><td>0</td><td>0</td><td>Q</td></tr>
<tr><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>indeterminate</td></tr>
</table>
</td><td>
<table>
<tr><th>Q</th><th>Q+</th><th>S</th><th>R</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>X</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>X</td><td>0</td></tr>
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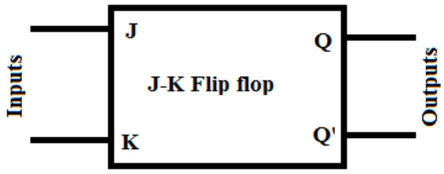
</td></tr>
<tr><td>JK flip flop



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<table>
<tr><th>J</th><th>K</th><th>Q+</th></tr>
<tr><td>0</td><td>0</td><td>Q</td></tr>
<tr><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>Q́</td></tr>
</table>
</td><td>
<table>
<tr><th>Q</th><th>Q+</th><th>J</th><th>K</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>X</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>X</td></tr>
<tr><td>1</td><td>0</td><td>X</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>X</td><td>0</td></tr>
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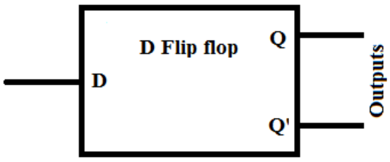
</td></tr>
<tr><td>D flip flop



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<table>
<tr><th>D</th><th>Q+</th></tr>
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<tr><td>1</td><td>1</td></tr>
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</td><td>
<table>
<tr><th>Q</th><th>Q+</th><th>D</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
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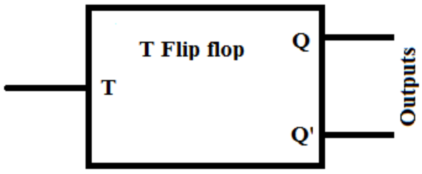
</td></tr>
<tr><td>T flip flop



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<table>
<tr><th>T</th><th>Q+</th></tr>
<tr><td>0</td><td>Q</td></tr>
<tr><td>1</td><td>Q́</td></tr>
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</td><td>
<table>
<tr><th>Q</th><th>Q+</th><th>T</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
</table>
</td></tr>
</table>

Where S,R, J,K,D and T – Flip flop inputs, Q- Present state and Q+ - Next state of the flip flop

Mathematical Representation Of Synchronous Sequential Circuit:

Q(t+1)=f{Q(t),x(t)}
Z(t)=g{Q(t),x(t)} for Mealy model
Z(t)=g{Q(t)} for Moore model
where Z(t) = output, Q(t) = present state, x(t) = present input

Verilog HDL SYNTAX:

Description	Syntax	Remarks
Initial Statement	Initial [timing_control] procedural_statement	Behavioral modeling
Always Statement	always [timing_control] procedural_statement	Behavioral modeling
Module instantiation statement	Module_name instance_name(port_association);	Structural modeling

Port association statement	Port_expr .portname (port_expr)	Structural modeling
NMOS & PMOS Verilog modeling	nmos n1(out,data,control); Pmos p1(out, data,control);	Switch level modeling

Verilog test bench	Module name_tb;
	// input declaration;
	//output declaration;
	//instantiate the unit under test(UUT)
	initial
	begin
	//input stimuli
	end
	endmodule
		Verilog test bench

Task	Task task_name Input arguments Output arguments Inout arguments Task decalartions Local variable declarations Begin Statements end endtask	Mixed style modeling
Functions	function [range or type] function name input declaration other declarations begin statement end endfunction	Mixed style modeling
User defined primitive	primitive udp_name(output,input); output declarations; input declarations; initial table state table entries endtable endprimitive	User defined primitive(UDP)
Altera FPGA	AND array: Programmable OR array : Fixed	Programmable array logic (PAL)