Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

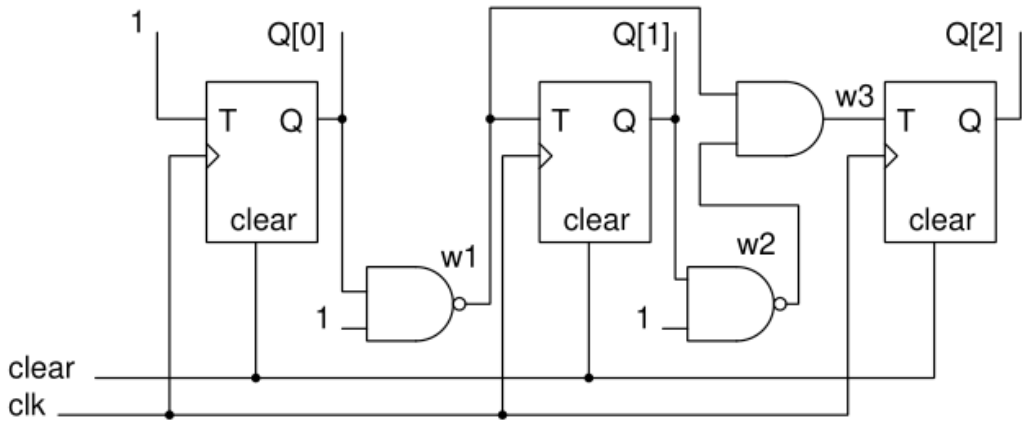
(A constituent unit of MAHE, Manipal)

THIRD SEMESTER BTECH. (E & C) DEGREE PROCTORED ONLINE EXAMINATION
JANUARY 2022
SUBJECT: DIGITAL SYSTEM DESIGN (ECE - 2153)

TIME: 75 min (9.20 AM to 10.35 AM) **MAX. MARKS: 20**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.
- Answer script must be a single pdf, good visibility of all texts and numbers.
- Name the file as: **RegistrationNumber_ECE2153_27_JAN2022**
- Upload correct pdf properly named well before 10.45 AM.

Q.No.	Questions
1A	Write a structural Verilog code for the circuit shown in **FigQ1A**. Use the names given in tha same figure.  **FigQ1A**
1B	Write a Verilog behavioural code for a 4-bit universal shift register which performs following tasks depending on select lines S_1S_0. **S_1S_0** **Task** 00 Hold 01 shift right 10 left shift 11 Parallel load
1C	Write a Verilog code for a 2:1 MUX using 'assign' statements and a testbench to generate all possible test vectors for the above MUX and observe the corresponding outputs.
	[4+3+3]
2A	Consider a synchronous sequential circuit with one input x, two D flip-flops and one output z. The excitation equations are $D_1 = \bar{x}\overline{Q_2} + \overline{Q_1}Q_2$ $D_2 = x\overline{Q_1} + \overline{Q_1}Q_2$

	$z = \bar{x} Q_1 + \overline{Q_1} x \overline{Q_2}$ Write Next state table, Excitation table, State table and State diagram for the above mentioned sequential circuit.
2B.	Design a ripple decade down counter [1001, 1000, 0111, 0110, 0101, 0100, 0011, 0010, 0001, 0000, 1001...] using positive edge triggered T flip-flops. Assume T flip flops have active low asynchronous clear signal.
2C.	Write Next state table, Excitation table and derive characteristic equation for a flip-flop with 2 inputs L & M and one output N. The truth table of the flip-flop is given below. Where N^+ indicates next state of N. **L M N^+** 0 0 1 0 1 complement of N 1 0 N 1 1 0
	[4+3+3]