MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

III SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)
MAKEUP EXAMINATIONS, APRIL 2022

DIGITAL SYSTEM DESIGN [ELE 2152]
REVISED CREDIT SYSTEM

Time: 2.00 PM-5.00 PM **Date: 23 April 2022** **Max. Marks: 50**

Instructions to Candidates:
- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. A bank door has three locks with a different key for each lock. Each key is owned by a different person. To open the door at least two people must insert their keys into the assigned locks. If there is a key inserted into lock it generates a high signal. Write a Boolean equation for which the bank door should open. Implement the digital circuit using 2 input NAND gates. ***(04)***

1B. Design a circuit to implement 4 input EXOR gate using 4:1 multiplexers and residual gates. ***(03)***

1C. Simplify the following truth table using 3 variable VEM for each of the output functions.

(d- don't care, A, B, C, D-input variable, F1, F2- output variables)

A	B	C	D	F_1	F_2
0	0	0	0	0	1
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	1	1
0	1	1	0	0	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	d	1
1	0	1	0	d	1
1	0	1	1	d	1
1	1	0	0	d	1
1	1	0	1	d	0
1	1	1	0	1	0
1	1	1	1	1	0

(03)

2A. Simplify the following 5 variable Boolean expression using Quine-Mc-cluskey method

$$F(A,B,C,D,E) = \sum m(0,1,9,15,24,29,30) + d(8,11,31)$$ ***(04)***

2B. A network router allows multiple computers to send messages to each other. However, only a single computer can send a message at any one time, otherwise, there is a collision. Create a collision detection circuit for such a router. The circuit has a 3-bit input, tx1, tx2, tx3 with each bit indicating that the corresponding computer is transmitting (1=sending, 0=not sending). The output is a single bit, col, that should be 1 if a collision is detected or 0 otherwise. Implement the digital circuit using decoder and additional gates. ***(03)***

2C. Design an 8-bit adder/ subtractor circuit using 74LS283. ***(03)***

3A. Design divide by 10 counter using IC 74LS93 ***(04)***

3B. Design an asynchronous mod 16 counter using T flipflops ***(03)***

3C. Convert JK flip-flop to T Flipflop and design the circuit for the same. ***(03)***

4A. Design a Single circulating one logic, in a 4-bit counter

a. using IC74LS194

b. using D flipflops ***(04)***

4B. Design synchronous sequence generator circuit that generates the sequence 0-1-2- 4-9-3-7-0 using DFF. ***(03)***

4C. Realize the Boolean functions using PLA. f1(a, b) = ∑m (2,3), f2(a, b) = ∑m (0,3) ***(03)***

5A. Design and test a circuit that checks for the sequence 010 continuously in a data sequence using D Flip-Flop (Overlapping allowed). Implement the design with Moore machine. ***(04)***

5B. Implement a 2 input OR gate function using CMOS logic. ***(03)***

5C. Write the Verilog HDL code for a fulladder using data flow modeling style and gate level modelling style, compare both modelling styles. ***(03)***