# MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
*(A constituent unit of MAHE, Manipal)*

## III SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)
## END SEMESTER PROCTORED ON-LINE EXAMINATIONS

## JANUARY 2022

## DIGITAL SYSTEM DESIGN [ELE 2152]

REVISED CREDIT SYSTEM

**Time: 75 Minutes + 10 Minutes** **Date: 24 January 2022** **Max. Marks: 20**

**Instructions to Candidates:**

- Answer **ALL** the questions.
- Missing data may be suitably assumed.
- Time: 75 minutes for writing + 10 minutes for uploading.

**1A.** A combinational network with 4 inputs A, B, C, and D, 3 intermediate outputs X, Y and Z and two outputs P and Q is shown in Figure Q1A. M1 and M2 are both AND gates. Find the Boolean equation for X, Y and Z. Implement Y using 2:1 multiplexer/s and residual gates.

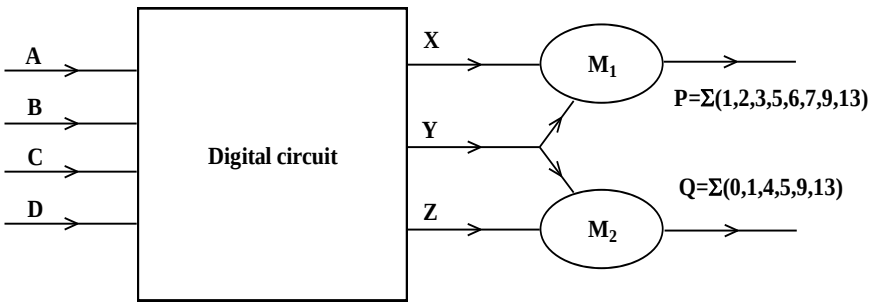



Figure Q1A

***(04)***

**1B.** A digital circuit has three inputs X, Y, and Z in which Y and Z are control signals. O is the output of the circuit. The functionality of the digital circuit is described by the below mentioned statements:

- Output O is same as input X when control signals Y and Z are the same.
- Output O is at logic level '1' when Y and Z are different.

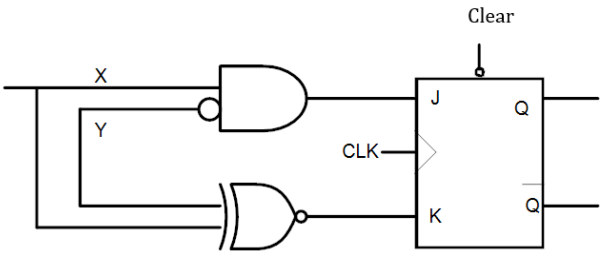
Realize the output using 3:8 decoder and necessary logic gate. ***(03)***

**1C.** Design a comparator circuit using 4 bit adder IC (74283 IC) and residual gates that compares two 4-bit unsigned numbers, $X_3$- $X_0$ and $Y_3$-$Y_0$. The comparator has two outputs: G and S. If X>Y output G=0, S=1; if X<Y output S=0 and G=1; if X=Y output G=S=0. ***(03)***

**2A.** An XY Flipflop is constructed from JK Flipflop as shown in the below.

a) Write an expression for X and Y
b) Derive the excitation table and characteristic equation for XY Flipflop.

***(03)***




**2B.** Write the state table representation of the FSM with the Flip-Flop input equations and output decoder equations

$$T1=Q_2x \quad ; \quad T2=x \quad ; \quad Z=Q_1Q_2$$

where T1 and T2 are the T flip flop inputs, x is the external input, z is the external output, $Q_1$ and $Q_2$ are the flip flop states.

Draw the state diagram of the FSM from the state table. Draw the complete circuit diagram of the FSM with Next State Decoder and Output Decoder as 4 to 1 mux, consider flip flop states as the select input of the multiplexer. ***(04)***

**2C.** Consider the functions $f_1(a, b, c)= \pi M(1,2,4,5,7)$ and $f_2(a, b, c)= \pi M(1,3,6,7)$. Show how it can be realized using Programmable Logic Array. ***(03)***