**DEPARTMENT OF MECHATRONICS**

**III SEMESTER B. TECH MECHATRONICS**

***MAKE UP EXAM***

**Subject: Digital System Design** **Subject Code: MTE 2152**

**Time: 2.00 to 5.00 pm** **Date:**

| Q. No. | | M | CO | PO | LO | BL |
|---|---|---|---|---|---|---|
| **1A** | Obtain a minimal SOP expression using Tabular method for the following equation. $F(A,B,C,D)=\sum m(2,4,7,9,11,12,14)+d(0,5,6,13,15)$ | **5** | **CO1** | PO1, PO3, PO12 | 1, 7, 13 | 2, 3 |
| **1B** | Design a 4 to 2 Priority Encoder. | **3** | **CO2** | PO1, PO2, PO3, PO12 | 2, 7, 9, 13 | 2, 3 |
| **1C** | Implement, 4-bit addition and subtraction operation using IC 74LS283 | **2** | **CO2** | PO1, PO2, PO3, PO12 | 2, 7, 9, 13 | 2, 3 |
| | | | | | | |
| **2A** | Design a circuit using 74LS283 that will perform two digit BCD addition | **4** | **CO2** | PO1, PO2, PO3, PO12 | 2, 7, 9, 13 | 2, 3 |
| **2B** | Design a presettable counter which can count the states 9,10 ,11,12,13,14,15 using JK Flip Flops. | **3** | **CO3** | PO1, PO2, PO3, PO12 | 3,7, 8,9, | 2, 3 |
| **2C** | Draw the state diagram for a Mealy machine, to detect the sequences 01011, 10100 and 11011 in a continuous data stream. | **3** | **CO3** | PO1, PO2, PO3, PO12 | 3,7, 8,9, | 2, 3 |
| **3A** | Design an Asynchronous Mod 8 counter using JK flip flop. Draw the waveforms at each flipflop to show the entire count. | **5** | **CO3** | PO1, PO2, PO3, PO12 | 3,7, 8,9, | 2, 3 |
| **3B** | Design a 4 bit Johnson Counter using D flip flops. | **3** | **CO3** | PO1, PO2, PO3, PO12 | 3,7, 8,9, | 2, 3 |
| **3C** | What is Race Around condition? Explain | **2** | **CO3** | PO1, PO2, PO3, PO12 | 3,7, 8,9, | 2, 3 |
| **4A** | Design a synchronous Modulo-10 up/down counter using T Flip flops | **4** | **CO3** | PO1, PO2, | 3,7, 8,9, | 2, 3 |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | | PO3, PO12 | | |
| **4B** | Realize f(X,Y,Z) = ∑m(0,2,3,5) using a 4 to 1 mux. | **4** | **CO2** | PO1, PO2, PO3, PO12 | 2, 7, 9, 13 | 2, 3 |
| **4C** | Illustrate the dataflow Verilog code for a single bit full adder. | **2** | **CO5** | PO1, PO5, PO12 | 6,7,8 ,18 | 2, 3 |
| **5A** | What is FPGA?, Explain how FPGA is different from ASIC? | **4** | **CO4** | PO1, PO3, PO7, PO12 | 3,7, 8,13 | 2, 3 |
| **5B** | Explain the different types of Registers used in sequential circuits. | **4** | **CO3** | PO1, PO2, PO3, PO12 | 3,7, 8,9, | 2, 3 |
| **5C** | Illustrate the structural Verilog code for a single bit full Subtractor. | **2** | **CO5** | PO1, PO5, PO12 | 6,7,8 ,18 | 2, 3 |