MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

FIFTH SEMESTER B. TECH (ELECTRONICS AND INSTRUMENTATION)

PROCTORED ONLINE MAKE-UP EXAMINATION - Feb/March. 2022

SUBJECT: **MICROCONTROLLERS (ICE 3152)**

TIME: 75 minutes **DATE: 24-02-2022** **MAX.MARKS:30**

Note: Answer *All* questions.

PART A

1. A general-purpose microprocessor normally needs which of the following devices to be attached to it?
    a. RAM
    b. ROM
    c. I/O
    d. All of the above

2. What is the duty cycle created by the following program:

```
BACK : SETB P1.3
LCALL DELAY
LCALL DELAY
CLR P1.3
LCALL DELAY
SJUMP BACK
```

    a. 33%
    b. 50%
    c. 66%
    d. 75%

3. Which 8051 ports need pull-up resistors to functions as an I/O Port?
    a. P0
    b. P1
    c. P2
    d. P3

4. Reset value of the 8051 P1 register is
    a. 00

b. 07
c. AA
d. FF

5. The machine cycle for 8051 if the XTAL frequency is 22MHz is
   a. 45.45ns
   b. 545.4ns
   c. 181.8ns
   d. 454.45ns

6. The timer's clock frequency for an 8051 microcontroller using a 16MHz clock is
   a. 1 MHz
   b. 1.33 MHz
   c. 921.6 KHz
   d. 133.6 KHZ

7. What is the delay generated by the DELAY subroutine in the program below. Assumer XTAL = 11.0592MHz, with the configuration of Timer 0, mode 1 and TH = FFF2H.

```
DELAY : SETB TR0
AGAIN : JNB TF0, AGAIN
        CLR TR0
        CLR TF0
        RET
```

   a. 15.19 us
   b. 30.38 us
   c. 60.76 us
   d. 121.52 us

8. If TH1 = FCH to obtain a baud rate of 9600, XTAL1 is
   a. 16 MHz
   b. 22 MHz
   c. 11.0592 MHz
   d. 25 MHz

9. What is the frequency generated by the following program assuming XTAL = 22MHz

```
MOV TMOD, #10H
```

```
BACK : MOV TL1, #0F7H
MOV TH1, #0FFH
SETB TR1
AGAIN: JNB TF1, AGAIN
CLR TR1
CPL P2.3
CLR TF1
SJMP BACK
```

a. 25 KHz
b. 50 KHz
c. 75 KHz
d. 100 KHz

10. In the instruction MOV TH1, #-200, find the hex value for the TH1 register
    a. -38
    b. 38H
    c. -38H
    d. 38

11. Indicate the selection made in the statement "TMOD = 0x20"
    a. Timer 1, mode 0, 16-bit
    b. Timer 1, mode 1, 8-bit autoreload
    c. Timer 2, mode 0, 16-bit
    d. Timer 2, mode 2, 8-bit autoreload

12. If XTAL = 11.0592MHz, the frequency used by the timer to set the baud rate is
    a. 921.6 KHz
    b. 56.6 KHz
    c. 28.8 KHz
    d. 550 KHz

13. What is the status of CY, AC, and P flags after the following instructions.

```
MOV A, #9CH
ADD A, #64H
```

a. CY =0; AC = 1; P = 1
b. CY = 1; AC = 0; P = 0
c. CY = 1; AC = 1; P = 0
d. CY = 0; AC = 0; P = 1

14. With SMOD = 1 and TH1 = -3, the baud rate obtained is 38 KHz. The crystal frequency used is
    a. 16 MHZ
    b. 22 MHZ
    c. 11.0592 MHZ
    d. NONE OF THE ABOVE

15. LJMP Main is used to bypass the memory space allocated to
    a. Scratch pad
    b. Stack
    c. IVR
    d. PC

16. As per data sheet of the 8051, for successful latching of the INT0, the pin must be held low until
    a. The execution of RETI instruction
    b. For one machine cycle
    c. Till ISR starts to execute
    d. Throughout the execution of the program

17. If a serial communication system has only a transmitter and a receiver connected by a single line, such a system is called
    a. Simplex
    b. Half Duplex
    c. Full Duplex
    d. Mutltiplex

18. Find a number that, when XORed to the A register, results in the number 2Eh in A.

```
MOV R0, A
XOR A, #2Eh
------------
```

    a. XOR A, R0
    b. XOR R0, A
    c. MOV A, R0
    d. MOV R0, A

19. Which of the following instruction is not correct
    a. JMP @A+DPTR
    b. ACALL LOOP

c. JNB P1.3, LOOP
d. JMP @A+PC

20. Which of the following is true
    a. The operation of RETI is to POP two bytes from the stack into the PC and reset the interrupt enable flip-flops.
    b. The operation of RETI is to POP two bytes from the stack into the PC and set the interrupt enable flip-flops.
    c. The operation of RETI is to POP three bytes from the stack into the PC and reset the interrupt enable flip-flops.
    d. The operation of RETI is to POP three bytes from the stack into the PC and set the interrupt enable flip-flops.
21. By using _____ instruction no flags of PSW are affected?
    a. ORL A, #20h
    b. PUSH DPL
    c. RR A
    d. All the given
22. Which of the following is correct
    a. ORL instruction is used to mask the status of the bits
    b. ORL C, /b alter the addressed bit b
    c. INC instructions that operates on the port direct address alter the latch for that port
    d. All the given
23. The value sent to the DAC (in decimal) for an angle 90 degree, while generating the sine wave is
    a. 255
    b. 128
    c. 192
    d. 0
24. Which of the following is true
    a. By modulating the width of the pulse applied to DC motor, we can increase or decrease the motor speed.
    b. Reset is a non-maskable active high interrupt line
    c. 8051 does not have dedicated internal hardware for PWM generation
    d. All the given

25. When 4*4 keyboard matrix is connected to 8051, which of the following correct step sequences are used to detect the key that is being pressed.

i) Check whether key is pressed or not

ii) Masking of bits

iii) Ensure all keys are released initially

a. i) iii) ii)
b. ii) i) iii)
c. iii) ii) i)
d. ii) iii) i)

26. Which of the following is not true in case of 8051

a. JB and JNB cannot be used for any bits of I/O ports 0, 1, 2, and 3
b. ANL can be used to read the content of an internal port latch
c. Using the instruction JNB P1.5, LOOP assumes that bit P1.5 is an input
d. All the given

27. Which of the following is true for ARM

a. A code area is usually read-only area
b. The program written in ARM assembly language can be assembled in a PC with different processor
c. Thumb instructions are either 16 or 32 bits long
d. All the given

28. Which of the following is not true for ARM

a. In FIQ mode R8-R14 are replaced by another set of registers which are suffixed by FIQ
b. Having register R13, helps to reduce the delay associated with call and interrupt
c. ARM has 37 registers each of which is 32 bits long
d. Most of the tasks run under unprivileged mode of ARM

29. Which of the following is true for ARM

SPSR is available for all the operating modes of ARM
Besides exceptions, processors can also be interrupted by instructions
ARM has 107 general purpose registers
All the given

30. Calculate the execution time for the following subroutine (assume time period for 1 machine cycle is 2 microsec)

Instruction	No.of machine cycle
MOV R3,#04H	1
LOOP3:MOV R2, #0F5H	1

```
LOOP2:MOV R1, #0FFH          1
LOOP1:DJNZ R1, LOOP1         2
      DJNZ  R2, LOOP2        2
        DJNZ   R3, LOOP3     2
        RET                  2
```

a. 1 second
b. 1.5 second
c. 2 second
d. 0.5 second

****