# INTERNATIONAL CENTRE FOR APPLIED SCIENCES
# MAHE, MANIPAL
## B.Sc. (Applied Sciences) in Engg.
## End – Semester Theory Examinations – NOV 2021
## III SEMESTER - SWITCHING CIRCUITS AND LOGIC DESIGN (ICS 232)

**Time: 3 Hours** **Date: 22 NOV 2021** **Max. Marks: 50**

- ✓ **Answer ALL questions.**
- ✓ **Missing data, if any, may be suitably assumed.**

**1** **A** Simplify the following expressions using algebraic manipulation.
g(a,b,c,d)=a'c'd'+a'bd+bcd+acd'+b'cd'

**B** Write the prime implicants, essential prime implicants and simplified expresion for the following function.
F(a, b, c, d)= ∑m(1, 3, 4, 5, 10, 11, 12, 13, 14, 15)

**C** Find the minimum cost SOP and POS expression for the following function using K-map and design the circuit using only NOR gates.
F(w, x, y, z)= ∑m(0, 1, 3, 4, 7, 11, 13, 15)+D(9, 12, 14)

**(2+4+4)**

**2** **A** Design a 3-bit binary to grey code converter using a decoder and other necessary gates. Write the truth table of the code converter and the decoder used in your design. Write the Verilog code for the same.

**B** Write the two cases where correction has to be made during the addition of 2 BCD digits. Give examples. Using 4-bit binary adders, design the single digit BCD adder by deriving the expression for the above correction.

**(5+5)**

**3** **A** Implement three-input majority function using 2-to-1 MUX

**B** Design and Write Verilog code for a 4-to-16 decoder constructed using 2-to-4 decoders.

**(4+6)**

**4** **A** Design a counter with the following repeated nonbinary sequence: 0, 1, 2, 3, 4, 5, 6. Use JK flip-flops. Treat the unused states as a don't-care conditions.

**B** Draw the logic diagram of T flip flop. Write its characteristic table, characteristic equation, and excitation table.

**(6+4)**

**5** **A** i) Discuss PLA with a neat logic diagram.
ii) Define a tri-state buffer. Write its truth table.

**B** Explain the following with a neat diagram for each.
i) NMOS realization of a AND gate.
ii) NOT Gate built using NMOS Logic **((4+2)+(2+2))**

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