MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

I SEMESTER M. TECH (POWER ELECTRONICS AND DRIVES)
END SEMESTER ON-LINE PROCTORED EXAMINATIONS
FEBRUARY 2022

EMBEDDED SYSTEM DESIGN [ELE 5171]

REVISED CREDIT SYSTEM

Time: 75 Minutes + 10 Minutes **Date: 09 February 2022** **Max. Marks: 20**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.
- Time: 75 minutes for writing + 10 minutes for uploading.

1A. Write an ARM7 subroutine to obtain ASCII code for both the nibbles of an 8-bit binary number passed to subroutine through D7 - D0 bits of R0 register. Return the result through R1, and R2 registers. ***(03)***

1B. Design an interfacing circuit to interface two common anode 7-segment LED display devices to mbedNXPLPC1768 microcontroller. Use GPIO pins p6 to p13 and p21 to p28 for the interface. Write a 'C' program to display numbers '00' to '99' continuously on the display devices with a delay of 1.25 sec between each display. ***(03)***

1C. Explain the following with respect to pre fetch abort exception.

i. When does this exception occur?
ii. What is the main reason for having this exception in APM7TDMI?
iii. What is the expected operation in pre fetch abort exception handler?
iv. Mention and describe the instruction used to return from pre fetch abort exception handler.
v. Discuss the reason for using this instruction to return. ***(04)***

2A. Develop a 'C' program for PIC16F877 microcontroller to configure the MSSP in SPI master mode to transmit data bytes 6BH and 7CH to slave device-1 connected to RA3 pin and data bytes 3EH and 2CH to slave device-2 connected to RA4 pin at 5 Mbps baud rate. Use idle state for clock as low level, transmit data on falling edge, sample input data at the middle of data output time. Take F_{osc} = 20MHz. ***(04)***

2B. With the help of a relevant timing diagram, explain PCI bus protocol for memory read operation to transfer three 8-bit data in the data field. Assume that target device takes two clock cycles to respond to address sent by initiator. No wait cycles are required in case of data-1. Target requests for two wait (extra) cycles during data-2 and initiator requests for one wait (extra) cycle during data-3. ***(03)***

2C. A real time system consists of four independent periodic tasks, T1 = (4,0.8), T2 = (5,1.8), T_3 = (20,4), and T4 = (2,0.3). Develop a suitable schedule using Rate monotonic algorithm for one hyperperiod. ***(03)***