Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

DEPARTMENT OF MECHATRONICS

I SEMESTER M.TECH. (INDUSTRIAL AUTOMATION AND ROBOTICS)

END SEMESTER EXAMINATIONS (PART-A), February 2022

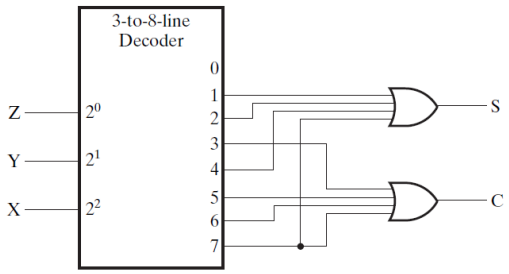
SUBJECT: ANALOG AND DIGITAL ELECTRONICS (Elective-1) [MTE 5001]

(Date: February 11, 2022)

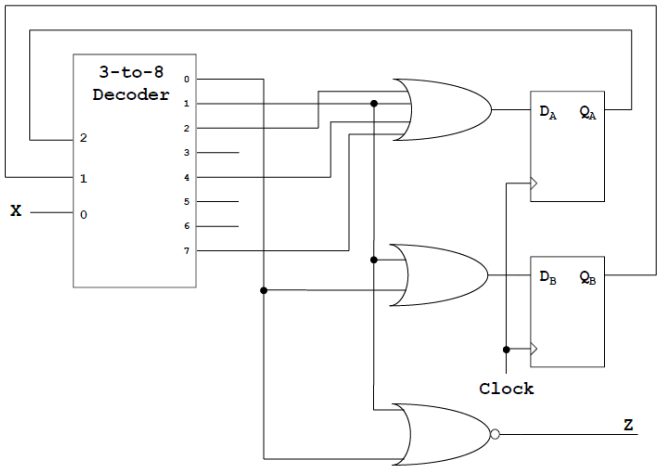
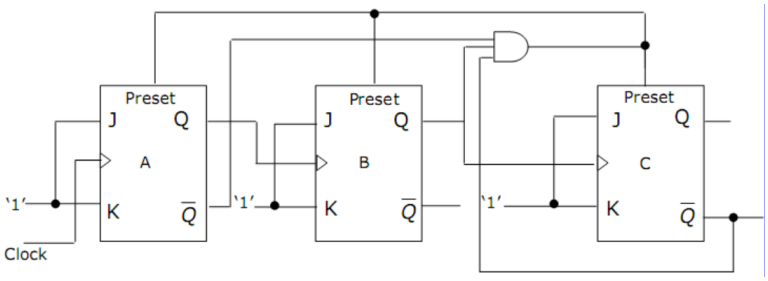
Time: 45 + 3 Minutes **MAX. MARKS: 30**

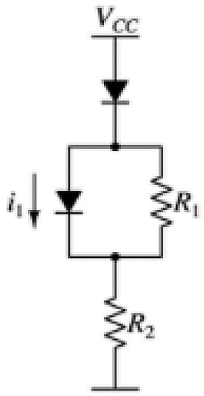
Instructions to Candidates:

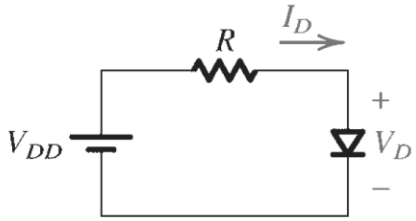
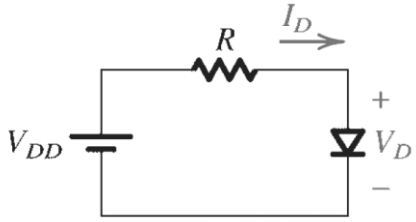
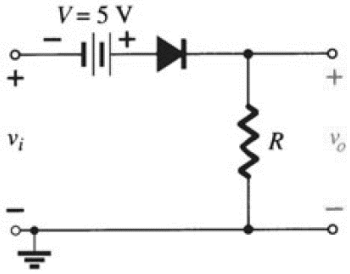
- Answer **ALL** the questions.

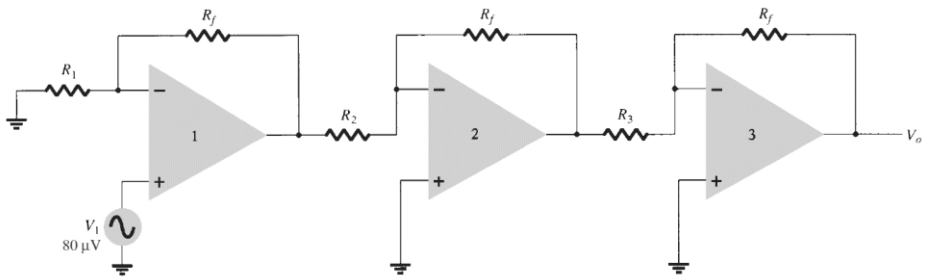
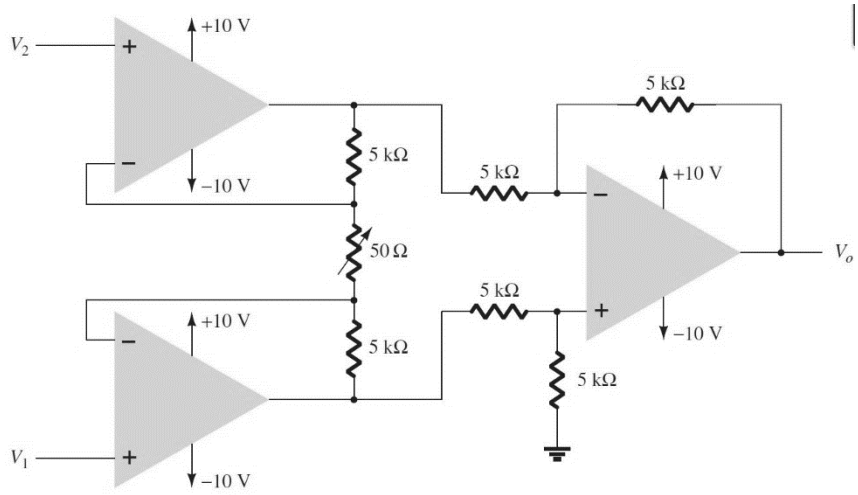
Q. No		M	CO	PO	LO	BL
	MCQ Type Questions (1 × 30 = 30)					
1.	**(10011001010) Excess 3 = (?) BCD** a) (110110010001) BCD b) (011110010100) BCD c) (000110010111) BCD d) (010001110111) BCD	**1**	**1**	**1**	**1**	**1**
2.	Analyse the below circuit and choose the correct expression of sum (S) and carry (C).  a) $S(X,Y,Z)=\sum m(1,2,3,4),\ C(X,Y,Z)=\sum m(5,6,7,0)$ b) $S(X,Y,Z)=\sum m(0,1,2,3),\ C(X,Y,Z)=\sum m(4,5,6,7)$ c) $S(X,Y,Z)=\sum m(1,2,3,7),\ C(X,Y,Z)=\sum m(4,5,6,7)$ d) $S(X,Y,Z)=\sum m(1,2,4,7),\ C(X,Y,Z)=\sum m(3,5,6,7)$	**1**	**1**	**1, 2, 4**	**1, 2**	**4**
3.	Consider the following functions- 1) F (A , B , C) = ∑ (0 , 2 , 3) 2) F (A , B , C) = ∑ (0 , 1 , 6 , 7) 3) F (A , B , C) = ∑ (0 , 1 , 2 , 4) 4) F (A , B , C) = ∑ (3 , 5 , 6 , 7)	**1**	**1**	**1**	**1**	**3, 4**

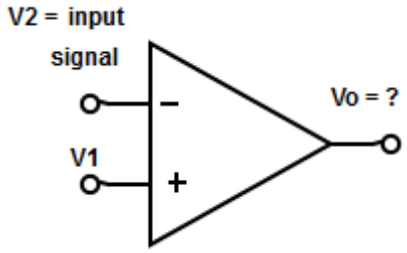
	Which of the above functions are **self-dual functions**? a) Only (3) b) Only (2) c) Only (3) and (4) d) All are self-dual functions					
4.	**Binary** and **hexadecimal representation of $(170.7)_8$ is**. (Use as many bits as needed, and approximate the fraction to 4 binary digits) a) Binary: 100110110.000 ; Hexadecimal: 87.E b) Binary: 001111000.111 ; Hexadecimal: 78.E c) Binary: 000111000.011 ; Hexadecimal: 87.F d) Binary: 100110000.010 ; Hexadecimal: 78.F	**1**	**1**	**1**	**1**	**1**
5.	Determine the **radix R** that satisfies the following: $(365)_R = (194)_{10}$. a) 5 b) 6 c) 7 d) 8	**1**	**1**	**1**	**1**	**1**
6.	Which gates in Digital Circuits are required to convert a NOR-based SR latch to an SR flip-flop? a) Two 2 input OR gates b) Two 3 input AND gates c) Two 2 input AND gates d) Two 3 input OR gates	**1**	**2**	**1**	**1**	**1**
7.	Consider the following statements for the Mealy model of Finite State Machine- 1) Outputs are a function of states only 2) Outputs are a function of external inputs and states 3) Outputs are usually specified on the states (in the circles) 4) Outputs are usually specified on the state transition arcs Which of the above statement(s) is/are correct for the **Mealy model** of FSM? a) Only (2) and (4) b) Only (3) c) Only (1) and (2) d) All statements are correct	**1**	**2**	**1, 2**	**1, 2**	**1**
8.	What will be the **number of outputs** produced by the combinational circuit that are designed to perform addition and subtraction? If the combinational circuit accepts two 2-bit unsigned numbers $C = C_1C_0$ and $D = D_1D_0$. The circuit produces C – D when C > D, and produces C + D otherwise. a) 2 b) 3 c) 4 d) 5	**1**	**2**	**1, 2**	**1, 2**	**3, 4**
9.	Analyse the below circuit and choose the correct answer from the following	**1**	**2**	**1, 2**	**1, 2**	**3, 4**

	 a) The circuit is Mealy b) The circuit is Moore c) The circuit is Mixed of Moore and Mealy d) The circuit is neither Moore nor Mealy					
10.	Analyze the sequential circuit shown in the below figure, and determine the way it works.  a) Modulo -3 down counter b) Modulo -5 down counter c) Modulo-3 up counter d) Modulo -5 up counter	**1**	**2**	**1, 2, 3**	**1, 2**	**3, 4**
11.	A sequential circuit is designed using JK flip-flops that will work as 4-bit modulo-16 ripple counter. If the propagation delay of each flip-flop is 60 nanoseconds, the **maximum clock frequency** that can be used is equal to _____ . a) 20 MHz b) 10 MHz c) 5.17 MHz d) 4.17 MHz	**1**	**2**	**1, 2**	**1, 2**	**1, 3**
12.	The nibble 1101 is storing in a bidirectional four-bit shift register. Its input is HIGH. The nibble 1011 is waiting to be entered on the serial data-input line. After **three clock pulses**, the shift register is storing _____. a) 1011 b) 1101 c) 0111 d) 1110	**1**	**2**	**1, 2**	**1, 2**	**2, 3**
13.	Consider the following statements for the Ring shift counter -	**1**	**2**	**1**	**1, 2**	**1**

	1) A sequence of equally spaced timing pulses may be easily generated 2) Clearing one flip-flop and presetting all others 3) Presetting one flip-flop and clearing all others 4) Presetting all the flip-flops Which of the above statement(s) is/are correct for the **Ring shift counter**? a) Only (2) and (4) b) Only (3) c) Only (1) and (3) d) All statements are correct					
14.	How many flip-flops are required in designing of four-bit up-down counter? a) 2 b) 3 c) 4 d) 5	**1**	**2**	**1, 2**	**1**	**1, 3**
15.	An 8-bit binary ripple UP counter with a modulus of 256 is holding the count 01111111. What will be the count after **135 clock pulses**? a) 0000 0101 b) 1111 1001 c) 0000 0110 d) 0000 0111	**1**	**2**	**1, 2**	**1, 2**	**1, 3**
16.	What is main requirement for **n-channel** to form in n-channel MOSFET? a) The voltage across the "oxide" layer must be less then threshold voltage (V_t). b) The voltage across the "oxide" layer must exceed threshold voltage (V_t). c) The voltage across the "oxide" layer must be equal to threshold voltage (V_t). d) The voltage across the "oxide" layer must exceed overdrive voltage (V_{OV}).	**1**	**3**	**1**	**1**	**1**
17.	In the circuit below, R_1 and R_2 are 4.4 and 1.1 kilo-ohms respectively. The voltage V_{CC} is 4.9 volts. The diode follows the standard diode equation, with Is of 16×10^{-12} milli-amperes, and the thermal voltage v_T of 25 milli-volts. (Assume, if both diodes are ON, the drops across them would be 0.65 volts each).  **What is the current i_1 (in milli-amperes)?**	**1**	**3**	**1, 2**	**1, 2**	**2, 3**

	a) 3.42 b) 2.97 c) 3.27 d) 3.125					
18.	For the circuit shown on below figure with V_{DD} = 6 Volt and R = 2 kilo-ohms. Assume that the diode has a current of 1 mA at a voltage of 0.7 V.  **The current I_D (in milli-amperes) is:** a) 4.3 b) 2.65 c) 4.65 d) 2.3	**1**	**3**	**1, 2**	**1, 2**	**2, 3**
19.	For the circuit shown on below figure with V_{DD} = 6 Volt and R = 2 kilo-ohms. Assume that the diode has a current of 1 mA at a voltage of 0.7 V.  **The diode voltage V_D (in Volt)is:** a) 0.725 V b) 0.5 V c) 0.6 V d) 0.625 V	**1**	**3**	**1, 2**	**1, 2**	**2, 3**
20.	In the circuit given below, 20 Volt peak sinusoidal input is applied. What will be the peak value of the output waveform?  a) 20 V b) 25 V c) 0 V d) -25 V	**1**	**3**	**1, 2**	**1, 2**	**3, 4**
21.	For an n-channel FET, what is the **direction of current flow**? a) Source to drain	**1**	**3**	**1**	**1**	**1**

	b) Drain to source c) Gate to source d) Gate to drain					
22.	How can inverting op amp be adapted to perform **integration**? a) Utilization of only resistor as feedback impedance. b) Utilization of only capacitor as feedback impedance. c) Utilization of very large resistor in parallel with the Capacitor as feedback impedance. d) Utilization of only inductor as feedback impedance.	**1**	**4**	**1, 2**	**1, 2**	**2, 3**
23.	Analyze the **output voltage** of an op-amp summing amplifier for the following voltages and resistors V_1 = -2 V, V_2 = +2 V, V_3 = +3 V, R_1 = 500 k ohms, R_2 = 500 k ohms, R_3 = 2 M ohms. Use R_f = 1.5 M-ohms in all cases. a) -7.15 V b) +3.65 V c) -2.25 V d) +2.25 V	**1**	**4**	**1, 2, 3**	**1, 2**	**3, 4**
24.	Analyze the circuit shown below and determine the **output voltage** for resistor components of value R_f = 450 k ohms, R_1 = 2.3 k ohms, R_2 =22 k ohms, and R_3 = 15 k ohms for an input of 80 microvolt.  a) -1.78 V b) +9.65 V c) -9.65 V d) +1.78 V	**1**	**4**	**1, 2, 3**	**1, 2, 3**	**4, 5**
25.	Analyze the circuit shown below and discover the **output voltage** expression  	**1**	**4**	**1, 2, 3**	**1, 2, 3**	**4, 5**

	a) $Vo = 21(V_1 - V_2)$ **b)** $Vo = 201(V_1 - V_2)$ **c)** $Vo = 21(V_2 – V_1)$ **d) None of the above**					
26.	Determine the **output Vo** from the following circuit  a) 180^o in phase with input signal b) 180^o out of phase with input signal c) Same as that of input signal d) Output signal cannot be determined	**1**	**4**	**1, 2, 3**	**1, 2, 3**	**4, 5**
27.	Which among the following can be used to detect the missing heart beat? a) Monostable multivibrator b) Astable multivibrator c) Schmitt trigger d) None of the mentioned	**1**	**5**	**1**	**1**	**1**
28.	Among which of the following factors do/does the operation of **sample and hold** mode depend/s? a) Input b) Output c) Position of switch d) All of the above	**1**	**5**	**1**	**1**	**1**
29.	How to obtain symmetrical waveform in **Astable multivibrator**? a) Use clocked RS flip-flop b) Use clocked JK flip-flop c) Use clocked D-flip-flop d) Use clocked T-flip-flop	**1**	**5**	**1**	**1**	**1**
30.	Which is not considered as a **linear voltage regulator**? a) Fixed output voltage regulator b) Adjustable output voltage regulator c) Switching regulator d) Special regulator	**1**	**5**	**1**	**1**	**1**

Reg. No.										

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DEPARTMENT OF MECHATRONICS

I SEMESTER M.TECH. (INDUSTRIAL AUTOMATION AND ROBOTICS)

END SEMESTER EXAMINATIONS (PART-B), February 2022

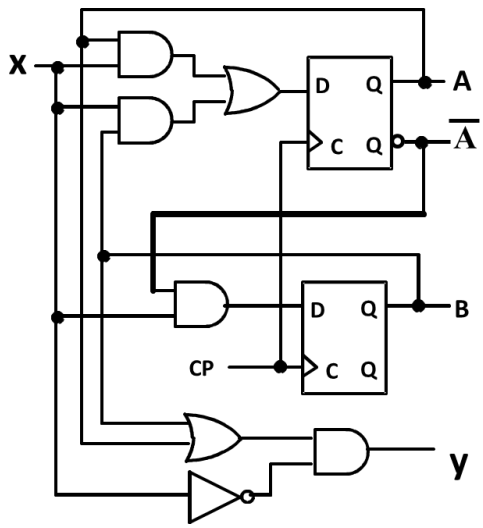
SUBJECT: ANALOG AND DIGITAL ELECTRONICS (Elective-1) [MTE 5001]

(Date: February 11, 2022)

Time: 75 + 10 Minutes **MAX. MARKS: 20**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data if any can be suitably assumed.

Q. No		M	CO	PO	LO	BL
	Descriptive Type Questions (10 × 2 = 20)					
1A.	Design a Finite State Machines (FSM) that receives BCD digits serially through input A_{in} and converts them to excess-3 digits and produces the result serially through output A_{out}. Assume an asynchronous reset input to reset the machine. The following is an example of some input and output streams: Input: A_{in} = 0 0 0 0 1 0 1 0 1 0 0 1 1 1 1 0 Output: A_{out} = 1 1 0 0 0 0 0 1 0 0 1 1 0 1 0 1 (i) Formulate the state diagram of the machine assuming a Mealy model. (ii) Construct the state table and state transition table of the FSM. (iii) Model the FSM using D flip flops and combinational logic.	**4**	**3**	**1, 3, 12**	**1, 3**	**3**
1B.	Analyze the sequential circuit given in Figure 1B and determine the way it behaves.  Figure 1B	**3**	**2**	**1, 3, 5**	**1, 2, 3**	**4, 5**

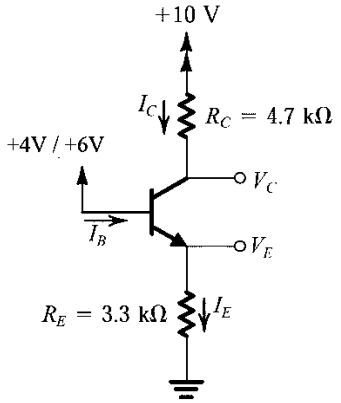
<table>
<tr>
<td>1C.</td>
<td>(i) Determine the decimal value (+55 and - 55) in binary using a total of 8 bits in the following notations:
<table>
<tr><td rowspan="2">Decimal</td><td colspan="3">Binary representation in 8 bits:</td></tr>
<tr><td>Signed-magnitude representation</td><td>Signed-1's complement representation</td><td>Signed-2's complement representation</td></tr>
<tr><td>+ 55</td><td></td><td></td><td></td></tr>
<tr><td>- 55</td><td></td><td></td><td></td></tr>
</table>
(ii) Assume the signed 2's complement arithmetic operation A - B in 6 bits. With B = 101101, the largest value allowed for A in order to avoid the occurrence of overflow is (_____)$_2$.</td>
<td>3</td><td>1</td><td>1, 12</td><td>1</td><td>3</td>
</tr>
<tr>
<td>2A.</td>
<td>Analyze the circuit shown in Figure 2A, and determine
(i) The mode of operation by considering +4 V and +6 V base voltages.
(ii) All node voltage and branch current for base voltage of +4 V.
Assume that β is specified to be 100.


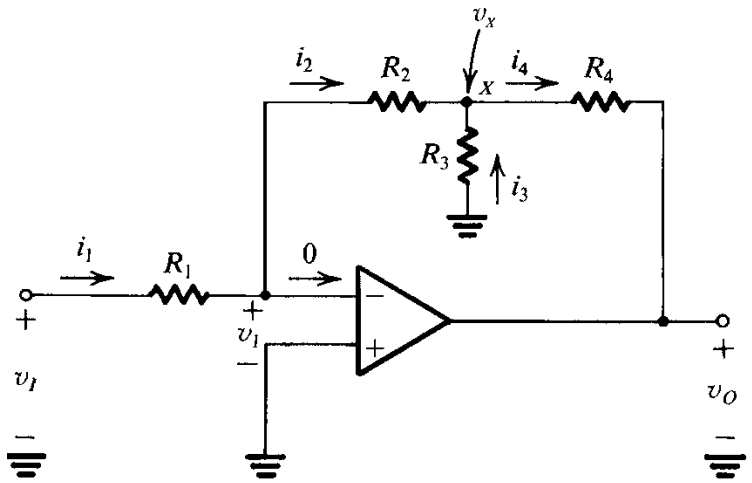
Figure 2A</td>
<td>4</td><td>3</td><td>1, 12</td><td>1, 2, 3</td><td>4, 5</td>
</tr>
<tr>
<td>2B.</td>
<td>Analyze the circuit shown in Figure 2B. By assuming the op-amp to be ideal perform the following.
(i) Derive an expression for the closed-loop gain v_O/v_I.
(ii) Design an inverting amplifier with a gain of 100 and an input resistance of 1 MΩ. Assume that for practical reasons it is required not to use resistors greater than 1 MΩ.


Figure 2B</td>
<td>3</td><td>4</td><td>1, 2, 4</td><td>1, 2, 3</td><td>4, 5</td>
</tr>
<tr>
<td>2C.</td>
<td>Build the free-running ramp generator by applying the concept of astable multivibrator.</td>
<td>3</td><td>5</td><td>1, 3, 12</td><td>1, 5</td><td>3</td>
</tr>
</table>