Question Paper

Exam Date & Time: 15-Feb-2021 (10:00 AM - 01:15 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

MANIPAL SCHOOL OF INFORMATION SCIENCES, MANIPAL
FIRST SEMESTER MASTER OF ENGINEERING - ME (EMBEDDED SYSTEMS) DEGREE EXAMINATION - FEBRUARY 2021

Advanced Computer Architecture [ESD 601]

Marks: 100 **Duration: 180 mins.**

MONDAY, FEBRUARY 15, 2021

Answer all the questions.

1) a. List out the difference between combinational and sequential Logic Circuits (5+5) (10)
b. Define the Significances of Data bus, Control bus and Address bus operations with respect to ARM and Harvard architecture. [TLO1.1]

2) Describe the merits and demerits of block-code encoding technique? Explain the key idea behind Huffman encoding technique with an example. [TLO2.1] (10)

3) Design a 4-bit 8-function arithmetic unit that will function as follows. [TO2.1] (10)

S2	S1	S0	Function F
0	0	0	2A
0	0	1	A plus B'
0	1	0	A plus B
0	1	1	A minus 1
1	0	0	2A plus 1
1	0	1	A plus B' plus 1
1	1	0	A plus B plus 1
1	1	1	A

4) Consider the following register transfer description. [TLO2.2] (10)

```
Declare registers     A [8], B [8], C [8], N [4];
Declare bus           Outbus [8];
START:    A ← 1, B ← 1, C ← 0; N ← 10;
          Outbus ← A;
LOOP:     Outbus ← B;
          If N = 0 then go to HALT;
          C ← A + B;
          A ← B;
          B ← C;
          N ← N – 1;
          Go to LOOP;
HALT:     HALT
```

Identify the components required in the processing unit, give their characteristics and design the processing unit incorporating the control points to perform the above task

5) With the help of neat block diagrams of the hardware, explain the two ways of generating timing (10)

	signals. Compare their advantages and disadvantages.[TLO2.2]	
6)	Write a ASM program to display "HELLO WORLD" using ARM instruction [TLO2.2]	(10)
7)	Define the Preindexing, Postindexing, Autoindexing operation taking place in the ARM, Explain with example. [TLO2.2]	(10)
8)	Explain the exception entry and return in ARM [TLO2.2]	(10)
9)	Define the necessity of interworking, also pipeline stage operations in ARM. [TLO2.2]	(10)
10)	List and explain the 4 schemes which helps to reduce branch hazards with example TLO3.1]	(10)

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