Exam Date & Time: 21-Apr-2022 (02:00 PM - 05:00 PM)

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

III SEMESTER B. TECH. (COMPUTER AND COMMUNICATION ENGINEERING) END SEMESTER MAKE-UP EXAMINATIONS, APRIL 2022

DIGITAL SYSTEMS AND COMPUTER ORGANIZATION [ICT 2171]

Marks: 50 **Duration: 180 mins.**

A

Answer all the questions.

Instructions to Candidates:
Answer ALL questions
Missing data, if any, may be suitably assumed

1) Design a code converter to convert a decimal digit represented in Gray code to a decimal digit represented in excess 3 code using only basic gates. (5)

A)

B) Perform $(12)_{10}$ x $(7)_{10}$ using Booth's multiplication algorithm. Indicate all the steps. (3)

C) The parameters of a computer memory system are specified as follows: Main memory size = 4K blocks, cache memory size = 512 blocks, block size = 8 words. Determine the size of the tag field of the main memory address under the following condition:

a. Fully associate mapping

b. Direct mapping (2)

2) Design a 4-bit sequential up counter using JK flipflop to count the sequences from 3 to 9 and all other states should reset to count 3. (5)

A)

B) Design a sequence detector circuit to detect the sequence 1101 from the input binary data stream. Also it should be capable to detect the overlapped sequences. (3)

C) Construct a T flip-flop using basic NOR latches. (2)

3) Using only JK - flip flops, design a MOD 10 counter circuit to generate an output waveform with 50% duty cycle. Using this, generate the sequence 0001111100. (5)

A)

B) Design 1 – bit magnitude comparator with cascading inputs using logic gates. Using the same, draw the circuit to compare two 4 – bit binary numbers. (3)

C) Design full adder using 74138IC and minimum external gates. (2)

4) Design a processing section for 4x4 Booth's multiplier. (5)

A)

B) Design a 4 – bit magnitude comparator using 7483 IC and external NOR gates only. (3)

C) Design 8:1 MUX using 2:1 MUXs only. (2)

5) Design a 4-bit binary Carry Look Ahead adder circuit. Discuss its merits over conventional 4-bit binary ripple carry adder. (5)

A)

B) Design a logic circuit to perform arithmetic operation F=XY when M=0 and perform F=X+Y when M=1 using minimum 74153ICs only. Assume X and Y are 1 – bit binary numbers and F is a 2 – bit binary number. (3)

C) Explain the operation of a Direct Memory Access System. (2)

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