Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

THIRD SEMESTER BTECH. (E & C) DEGREE PROCTORED ONLINE EXAMINATION
JANUARY 2022
SUBJECT: Computer Organization and Architecture (ECE - 2152)

TIME: 75 min (9.20 AM to 10.35 AM) **MAX. MARKS: 20**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.
- Answer script must be a single pdf, good visibility of all texts and numbers.
- Name the file as: RegistrationNumber_SubjectCode_dd_JAN2022
- Upload correct pdf properly named well before 10.45 AM

Q. No.	Questions	M*	C*	A*	B*
1A	Perform 448 ÷ 17 using restoring method with clear steps. Draw the flow chart.	4	CO2	C4	L5
1B	Compute the following (i) Convert $(-19.875)_{10}$ into its equivalent 32-bit IEEE floating-point format. (ii) Convert C009999A H IEEE floating-point number into its equivalent decimal value. (iii) Perform (-0.5 x 0.4375) using binary floating-point multiplication algorithm	3	CO2	C4	L2
1C	With the help of a diagram, explain the working principle of MAC unit in Digital signal processor. Write the significance of guard bits.	3	CO5	C2	L2
2A	Design an arithmetic unit of ALU for the following specifications. Here, A, B are four bit data and S0, S1 are select lines	4	CO1	C1	L6

S1	S0	Function
0	0	B - A
0	1	B + 1
1	0	2A
1	1	A - 1

2B.	Using the Hardwired control design approach, design the processing section with all the required control signals for the following register transfer description. Also, draw the complete logical diagram with counter and decoder; and also give the state diagram. Declare registers A[8], B[8], C[3], Inbus[8], Outbus[8]; START: A← 0, B← Inbus, C← 4; LOOP: A← A-B, C ← C-1; If C ‡ 0 then go to LOOP Outbus ← A; HALT: Go to HALT	3	CO4	C1	L6
2C.	Differentiate between the following (Mention 3 key differences for each) (i) RISC and CISC processors (ii) SIMD and MIMD processors	3	CO5	C2	L4

M*--Marks, C*--CLO, A*--AHEP LO, B* Blooms Taxonomy Level